ABSTRACT

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METHODOLOGY OF NETWORK ENVIRONMENT TESTING FOR IoT DEVICES

(p. 4 – 11)

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The article reviews methods and technologies for testing the network environment of embedded systems and writing test documentation. As an example, a testing technique based on a defect report has been developed. A performance test was developed to check the load of the embedded device's network environment using special bash scripts for performance testing.

***Keywords*:** IoT, embedded system, test case, defect report, troubleshooting, performance testing.

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ONE APPROACH TO ACCELERATE THE EXPONENTIATION ON GALOIS FIELDS FOR DATA PROTECTION CRYPTOGRAPHIC SYSTEMS

(p. 12 – 18)

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The new approach to accelerate the computational implementation of the basic for a wide range of cryptographic data protection mechanisms operation of exponentiation on Galois Fields have been proposed. The approach is based on the use of a specific property of a polynomial square and the Montgomery reduction. A new method of squaring reduces the amount of computation by 25% compared to the known ones. Based on the developed method, the exponentiation on Galois Fields procedure has been modified, which allows to reduce the amount of calculations by 20%.

***Keywords*:** multiplication operation on Galois fields, cryptographic algorithms based on Galois Fields algebra, Galois Fields exponentiation, Montgomery reduction.

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OPTIMAL CONSTRUCTION OF THE PATTERN MATRIX FOR PROBABILISTIC NEURAL NETWORKS IN TECHNICAL DIAGNOSTICS BASED ON EXPERT ESTIMATIONS

(p. 19 – 25)

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In the field of technical diagnostics, many tasks are solved by using automated classification. For this, such classifiers like probabilistic neural networks fit best owing to their simplicity. To obtain a probabilistic neural network pattern matrix for technical diagnostics, expert estimations or measurements are commonly involved. The pattern matrix can be deduced straightforwardly by just averaging over those estimations. However, averages are not always the best way to process expert estimations. The goal is to suggest a method of optimally deducing the pattern matrix for technical diagnostics based on expert estimations. The main criterion of the optimality is maximization of the performance, in which the subcriterion of maximization of the operation speed is included. First of all, the maximal width of the pattern matrix is determined. The width does not exceed the number of experts. Then, for every state of an object, the expert estimations are clustered. The clustering can be done by using the *k*-means method or similar. The centroids of these clusters successively form the pattern matrix. The optimal number of clusters determines the probabilistic neural network optimality by its performance maximization. In general, most results of the error rate percentage of probabilistic neural networks appear to be near-exponentially decreasing as the number of clustered expert estimations is increased. Therefore, if the optimal number of clusters defines a too "wide" pattern matrix whose operation speed is intolerably slow, the performance maximization implies a tradeoff between the error rate percentage minimum and maximally tolerable slowness in the probabilistic neural network operation speed. The optimal number of clusters is found at an asymptotically minimal error rate percentage, or at an acceptable error rate percentage which corresponds to maximally tolerable slowness in operation speed. The optimality is practically referred to the simultaneous acceptability of error rate and operation speed.

Keywords: technical diagnostics, probabilistic neural network, pattern matrix, expert estimations, clustering, performance maximization.

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VECTOR SPACE MODELS OF KYIV CITY PETITIONS

(p. 26 – 34)

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In this study, we explore and compare two ways of vector space model creation for Kyiv city petitions. Both models are built on top of word vectors based on the distributional hypothesis, namely Word2Vec and FastText. We train word vectors on the dataset of Kyiv city petitions, preprocess the documents, and apply averaging to create petition vectors. Visualizations of the vector spaces after dimensionality reduction via UMAP are demonstrated in an attempt to show their overall structure. We show that the resulting models can be used to effectively query semantically related petitions as well as search for clusters of related petitions. The advantages and disadvantages of both models are analyzed.

***Keywords*:** vector space model, FastText, Word2Vec, petitions analysis, UMAP.

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LOCAL FEATURE EXTRACTION IN IMAGES

(p. 35 – 47)

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The methods of the local feature point extraction are analyzed. The analysis shows that the most effective detectors are based on the brightness gradient determination. They usually use the Harris angle detector, which is complex in calculations. The algorithm complexity minimization contradicts both the detector effectiveness and to the high dynamic range of the analyzed image. As a result, the high-speed methods could not recognize the feature points in the heavy luminance conditions.

The modification of the high dynamic range (HDR) image compression algorithm based on the Retinex method is proposed. It contains an adaptive filter, which preserves the image edges. The filter is based on a set of feature detectors performing the Harris-Laplace transform which is much simpler than the Harris angle detector. A prototype of the HDR video camera is designed which provides sharp images. Its structure simplifies the design of the artificial intelligence engine, which is implemented in FPGA of medium or large size.

***Keywords*:** FPGA, feature extraction, HDR, pattern recognition, artificial intelligence.

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GIF IMAGE HARDWARE COMPRESSORS

(p. 48 – 55)

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Increasing requirements for data transfer and storage is one of the crucial questions now. There are several ways of high-speed data transmission, but they meet limited requirements applied to their narrowly focused specific target. The data compression approach gives the solution to the problems of high-speed transfer and low-volume data storage. This paper is devoted to the compression of GIF images, using a modified LZW algorithm with a tree-based dictionary. It has led to a decrease in lookup time and an increase in the speed of data compression, and in turn, allows developing the method of constructing a hardware compression accelerator during the future research.

***Keywords*:** FPGA, GIF, lossless compression, image compression, dictionary, hardware acceleration

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ARCHITECTURAL REVIEW AND CONCEPTUAL DEVELOPMENT OF FACULTY INFORMATION SYSTEM “KPI-CONNECT”

(p. 56 – 63)

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This paper is dedicated to development model of information system to automate educational process based on the Faculty of Informatics and Computer Science at NTUU “Igor Sikorsky Kyiv Polytechnic Institute”. Existing educational systems of different higher education institutions had been studied; main realized functions of similar platforms were defined. As a result of research model, that enables insertion of students, teachers and other university personnel data, storing personal data and information about users’ scientific works, and also is able to be integrated into existing university information space, has been obtained.

Keywords: educational process, information system, automatization, practical use.

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MICROCONTROLLER FOR THE LOGIC TASKS

(p. 64 – 72)

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A new SM16 microcontroller architecture is proposed which is intended for the logic-intensive applications in the field-programmable gate array (FPGA). The microcontroller has the stack architecture which provides the implementation of the most of instructions for a single clock cycle. The short but fast programs are derived due to the 16-bit instructions, which code up to three independent operations, and intensive use of the threaded code style. The framework is developed which compiles the program, simulates it, and translates to the ROM. The developed SM16 core with additional three-stack blocks, hash-table, and instructions that accelerate the execution of parsing operations is used for efficient XML-document processing and can be frequently reconfigured to the given document grammar set. The parsing speed equals to one byte per 24 clock cycles.

***Keywords*:** VHDL, XML, parser, FPGA, stack processor, grammar, FSM