ENSURING DYNAMIC STABILITY OF CONSTANT POWER LOADS IN FUTURE DC DISTRIBUTION POWER SYSTEMS USING ACTIVE DAMPING

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DC distribution is widely used in telecom and data centres, and it is envisioned to get wide acceptance in microgrid and buildings' power systems in the near future as a viable alternative to conventional AC systems. The main building blocks of DC power systems are switching power converters and rectifiers that have nonlinear characteristics. When the voltages are tightly regulated, the converters will act as constant power loads (CPLs). The CPL is known to exhibit the negative incremental impedance and may cause the dynamic instability of the system. The problem associated with CPLs is traditionally tackled using passive damping which has serious drawbacks such as increased size, decreased reliability and efficiency of the system. This paper introduces an active method to inject damping current into the power bus employing an auxiliary power circuit. The proposed approach ensures that the system operates with sufficient stability margin in a small-signal sense. Comparing with previous works, the advantage of the proposed damping circuit is that the absorbed energy for damping is transferred into a neighbouring bus with minimal energy losses.

AC-DC systems, constant power loads, DC distribution, DC power systems, dynamic stability, negative incremental impedance.

A typical DC distributed-energy-resources (DER) system, shown in Fig. 1(a), consists of switching-mode-power modules interconnected at the bus. This structure can achieve effective power distribution and overall system robustness independent from outages, increased power demand and component failures. Typical DC DER

systems are used for DC distribution in buildings [1], [2], telecom [3], [4], electric aircrafts [5], electric vehicles [6] and warships [7].

However, due to very fast control of power electronic converters, the dynamic interactions between various sources and loads modules may cause the degradation of system stability, as the modules are usually designed considering stand-alone operation [8]. Specifically, when a power converter feeds a constant power load (CPL), it exhibits negative incremental impedance behavior at its input terminals. A steady state V–I characteristic of CPL is depicted in Fig. 1(b). When the source voltage decreases, the current drawn by the load is increases, $dv/di < 0$, which results in negative incremental impedance and subsequent system oscillations and stability problems.

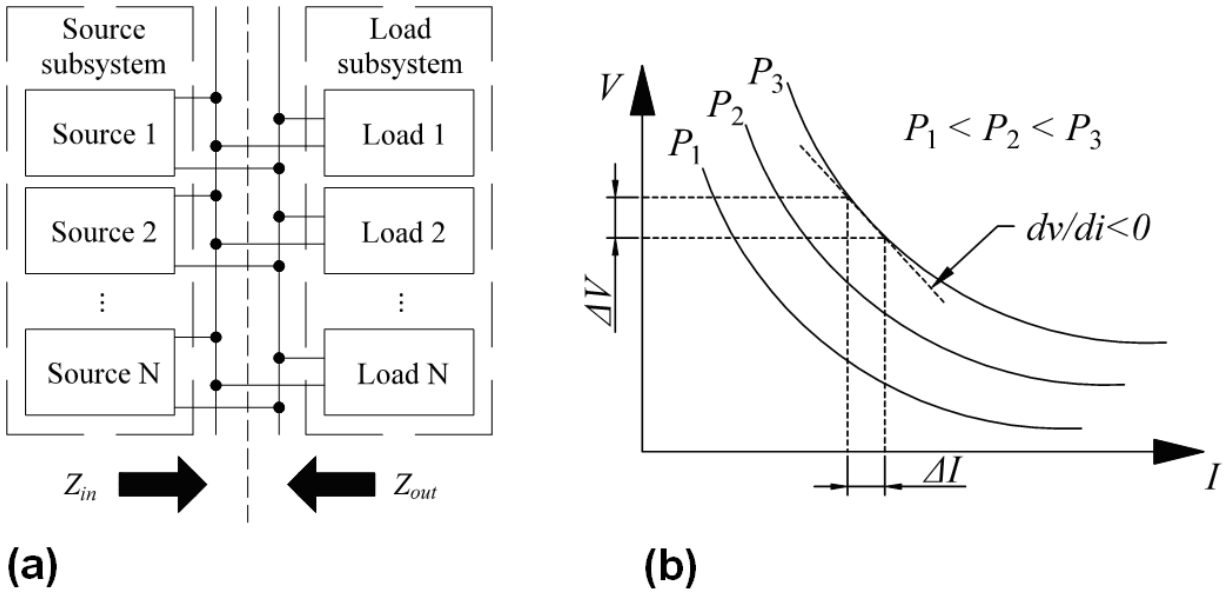


Fig. 1. A typical DC DER system: (a) its architecture; and (b) V-I characteristic to explain the negative incremental impedance of CPLs

In a DC power distribution system, there are many electronic loads, e.g. servers, which have floating power demands depending on the required computational load. Embedded step-down converters power motherboards of a server or other intelligent equipment. These converters will tightly regulate the output voltage regardless of fluctuations in the input voltage. As a result, when the input voltage decreases, the converter input current increases and vise versa, thus

exhibiting a negative incremental impedance characteristic of CPL in a small signal sense.

To employ the conventional linear theory for analyzing the CPL effects on system's stability, small signal models must be built using simplifications and linearization of the original system. Small-signal stability criterion was firstly developed and applied to the problem of input filter and converter inter-actions by Middlebrook in 1976 [9]. Using his methodology, the stability of a system can be observed through the ratio of source/load impedances, namely minor loop gain. Later, more sophisticated forbidden regions were developed to en-sure sufficient stability margin as summarized in [10].

The paradigm shift in power electronics that the communication between sources and loads will bring potential benefits on power managements is paving a path to optimization of DER systems feeding smart loads [11], [12]. It is envisioned that the future smart electronic loads will use active dampers to flexibly configure new systems and ensure the desired performance by using the information from smart loads.

In the framework of power-informing sources/loads, an auxiliary power circuit acting as a virtual RC damping filter is proposed for damping an unstable DER system with low energy loss. Small-signal analysis methods and stability criteria are used to calculate the required damping current. Finally, simulation studies based on the DC microgrid built by Alpha Technologies are performed to verify the proposed approach.

Small-Signal Impedance and Damping Methods: Based on impedance-based small-signal analysis, the DER system has to be divided into source and load subsystems as depicted in Fig. 2. Here, an ideal voltage source V_s in series with output impedance $Z_{out}(s)$ represents the actual power sources. The impedance $Z_{in}(s)$ in small-signal sense represents the actual loads. The equivalent small-signal circuit of the system in Fig. 1(a) is shown in Fig. 2. In [13] and [14] it was shown that the system of Fig. 2 is stable if and only if all of the following conditions are satisfied:

- The actual source is stable when unloaded

- The actual load is stable when powered from an ideal power source
- The system described by the transfer function

$$H(s) = \frac{V_l(s)}{V_s(s)} = \frac{1}{1 + \dfrac{Z_{out}(s)}{Z_{in}(s)}} \tag{1}$$

is stable. Here $H(s)$ is a closed loop transfer function with a minor loop gain $T_m(s) = Z_{out}(s)/Z_{in}(s)$. Therefore (1) will be stable when T_m satisfies Nyquist stability criterion, i.e. $|T_m| < 1$.

The most conservative stability criterion [9] requires that the source impedance Z_{out} is much smaller than the load impedance Z_{in} at all frequency ranges, i.e. $|Z_{out}(s)| << |Z_{in}(s)|$. This criterion basically ensures that the Nyquist plot of $T_m(s)$ stays within the unit circle with a sufficient gain margin. However, ensuring the system comply with this conservative criterion is not practical. Therefore, some forbidden-region criterions were proposed in [10] and [15] for reasonable estimations of the system's stability. The target of applying a damper is to reshape the output impedance Z_{out} and ensure that the final Nyquist plot of $T_m(s)$ is away from the forbidden region.

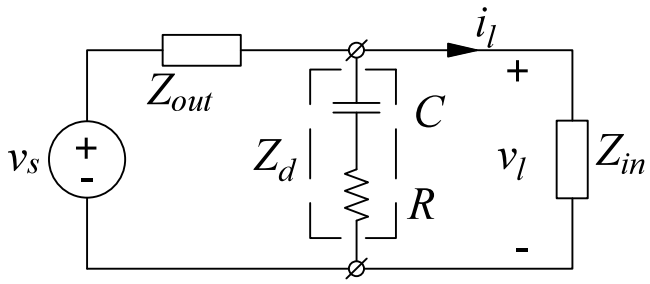


Fig. 2. Impedance based small-signal model of a typical bus feeding CPLs

Damper Approach to the CPL Instability: The small-signal impedance of CPL can be derived as

$$Z_{in} = \frac{dv_l}{di_l} = \frac{d}{di_l}\left(\frac{P_l}{i_l}\right) = -\frac{P_l}{i_l^2} = -\frac{v_l}{i_l} = -R_l. \tag{2}$$

Therefore, when CPL is connected to the source, the system will become negatively damped. In this situation, if the phase angle of Z_{out}/Z_{in} gets close to the dangerous $\pm 180^\circ$ zone and $|Z_{out}| > |Z_{in}|$ in high frequency region, the system will become unstable.

Application of passive damping may solve the problem of instability. This methodology is summarized in [16], where several damping techniques are discussed. It is noted that the paper gives a general design approach to stabilize the source with *LC* output filter which is modeled as a second-order impedance. However, a practical power system normally has a higher-order output impedance with more complicated characteristics. In addition, previous dampers need to be connected in parallel with the filter inductor *L* or in series across the source and load. In general, it can be challenging to apply the aforementioned dampers in realistic DERs. An *RC* damper can be directly connected in parallel with the power source terminals. In practical power supplies the damping is achieved by putting large electrolytic capacitors at the output terminals and the switching-ripple filter capacitor then becomes overdesigned. Moreover, the additional damping elements impact cost, weight and efficiency of the system.

RC Damper Achieved By Auxiliary Circuit: A method to calculate the parameters of an *RC* damper based on Routh-Hurwitz criterion has been proposed in [16]. This methodology can be potentially applied to higher order systems with numerical calculations [17]. In this section, we propose a hybrid method to derive the parameters of *RC* damper by applying both Forbidden region and Routh-Hurwitz criterion methodologies, respectively.

An *RC* damping circuit has two main parameters, *R* and *C*, which can be calculated by composing at least two independent equations. It is assumed that the system oscillation frequencies $s_1 = j\square_1$, $s_2 = j\square_2$, ... , $s_n = j\square_n$ are known and obtained through either eigenvalue or bode plot analysis. The system stability can be estimated from the open loop transfer function by using Nyquist criterion. According to this criterion and a given gain margin *GM*, the first set of equations can be outlined as

$$\begin{cases} \left| \dfrac{Z_{out}(s_1)\cdot Z_d(s_1)}{[Z_{out}(s_1)+Z_d(s_1)]/Z_{in}(s_1)} \right| \le \left| \dfrac{1}{GM} \right| \\ \cdots \\ \left| \dfrac{Z_{out}(s_n)\cdot Z_d(s_n)}{[Z_{out}(s_n)+Z_d(s_n)]/Z_{in}(s_n)} \right| \le \left| \dfrac{1}{GM} \right|. \end{cases} \tag{3}$$

In addition, the system stability can be evaluated applying the Routh-Hurwitz criterion to the closed-loop transfer function. Then we can get the second set of equations. Considering the damper impedance Z_d, the denominator of (1) becomes

$$D(s) = [Z_{out}(s) + Z_d(s)]/Z_{in}(s) + Z_{out}(s)\cdot Z_d(s). \tag{4}$$

For a given n-order-closed-loop system, the denominator of its transfer function can be expressed as

$$D(s) = d_n s^n + d_{n-1}s^{n-1} + \cdots + d_1 s + d_0. \tag{5}$$

A necessary but not sufficient condition for the system stability is that all polynomial coefficients of (5) must be positive. Then, the second group of equations will be

$$\begin{cases} d_n > 0 \\ d_{n-1} > 0 \\ \cdots \\ d_0 > 0. \end{cases} \tag{6}$$

In (3) and (4), the output impedance Z_{out} is expressed as a polynomial

$$Z_{out}(s) = \frac{a_n s^n + a_{n-1}s^{n-1} + \cdots + a_1 s + a_0}{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_1 s + b_0}, \tag{7}$$

where the parameters, a_0, a_1, …, a_n, and b_0, b_1, …, b_n, can be extracted using numerical methods. The damping circuit impedance Z_d is expressed as

$$Z_d(s) = \frac{RCs+1}{Cs}. \tag{8}$$

The small-signal impedance of an ideal CPL Z_l is given by (2). Finally, d_0, d_1, …, d_n

are derived using (2), (7) and (8), such that (6) becomes

$$\begin{cases} CR_l a_n - CRa_n + CRR_l b_n > 0 \\ R_l b_n - a_n - CRa_{n-1} + CR_l a_{n-1} + CRR_l b_{n-1} > 0 \\ R_l b_{n-1} - a_{n-1} - CRa_{n-2} + CR_l a_{n-2} + CRR_l b_{n-2} > 0 \\ \dots \\ R_l b_1 - a_1 - CRa_0 + CR_l a_0 + CRR_l b_0 > 0 \\ R_l b_0 - a_0 > 0. \end{cases} \tag{9}$$

The equations (3) and (9) can be solved for the damping-circuit parameters R and C such that both sufficient gain margin and partial Routh-Hurwitz criterion are satisfied. This hybrid method allows us to get appropriate values R and C with simplified calculations. Observing from (9), the system cannot be stabilized when

$$R_l < \frac{a_0}{b_0}. \tag{10}$$

Active Damping Circuit: An active auxiliary circuit can be designed to substitute a passive damper and generate the required damping current. A simplified circuit diagram that demonstrates the proposed concept is shown in Fig. 3, where an ideal current source is commanded the reference i^*. The command current will be generated according to the required damping impedance and the bus voltage. The active damping circuit can be realized using any bi-directional DC/DC topology. The element parameters and control loop should be selected to ensure the required damping and dynamic stability of the system for all frequencies of interest.

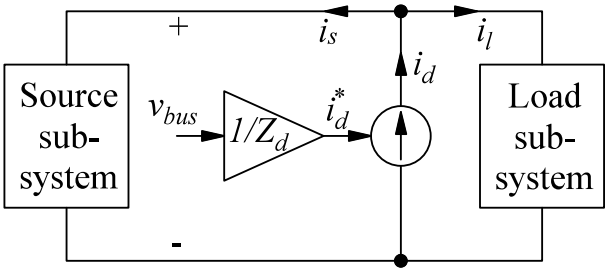


Fig. 3. Proposed approach depicting and ideal current source commanded to behave as a damping circuit with appropriate equivalent impedance

Load-informed Damping Circuit: When a smart damper circuit is aware of the impedances of sources and loads at the DC bus, it can be controlled in real time to

generate the optimal damping current. This strategy is depicted in Fig. 4 and can be realized through the following principles:

1) Each building block (source and load) of the DC DER system can communicate with the damping circuit.

2) Impedance characteristics will be extracted from source and load by manufacturers. This information with power level and consumed/supplied current will be filled into a two dimensional array shown in Table I.

3) The array will be sent to the damping circuit, before these devices are connected. In addition, the operating point of each source and load device and their equivalent impedances will be sent to the damping circuit in real time.

4) The equivalent source and load impedances Z_{out} and Z_{in} are calculated/update, and both open-loop and closed-loop gains are obtained.

5) The optimal damping parameters are derived by solving (3) and (9) in the auxiliary circuit.

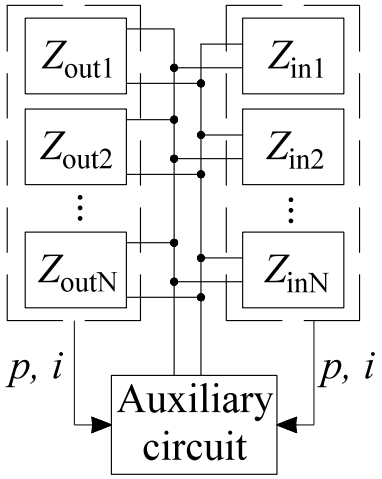


Fig. 4. Proposed approach for global active damping using auxiliary circuit

TABLE I: AN IMPEDANCE MATRIX FOR A TYPICAL BUILDING BLOCK OF A MICROGRID

	Power level		
Current level	Z_{11}	Z_{12}	Z_{13}
	Z_{21}	Z_{22}	Z_{23}
	Z_{31}	Z_{32}	Z_{33}

Alpha Microgrid and Proposed Circuit: Different active damping methods have been proposed in [18]–[23]. These works concentrated on reshaping the source or load impedances by control modifications. In addition, bidirectional circuits in [24], [25] only deal with net-zero energy as they need an extra capacitor to achieve energy storage. The proposed circuit will use a stiff bus as the energy source or storage element to provide the bipolar damping current. This concept is applicable to most of DC microgrids. The Alpha microgrid will be taken as an example to illustrate our design.

Alpha Technologies Ltd. has recently completed a 450 kVA energy management system (EMS) for a AC-DC DER network comprised of power converters and 1 MWh battery banks. The system is installed at three different locations on the UBC campus to shave the peak power demands from the buildings. At one of the locations, Kaiser Building, Alpha has provided a test bed consisting of 380 VDC, 48 VDC and 24 VDC buses. The system's photo and diagram are shown in Fig. 5 part (a) and (b), respectively. As seen from Fig. 5, the 380 VDC and 48 VDC buses have batteries connected to them. These batteries with very low impedance make these two buses very stiff. However, the 24 VDC bus may need a damper to enable connection of the CPLs. We built a model of 48-to-24 V DC/DC converter based on the parameters of CXDF 48-24/2kW. The total power capacity of this bus is 8 kW (with appropriate number of parallel-connected converters) and it can serve a combination of of DC loads within its rated output.

The proposed active damper circuit is shown in Fig. 6. To simplify the circuit design, a non-isolated buck-boost topology as defined in [26] is used here. This circuit does not need additional energy storage elements, as a stiff battery-powered 48 VDC bus is used to provide or observe the energy during damping. An isolated topology can be used when the galvanic isolation between two buses are needed. The inner-control loop operates in fixed frequency peak-current-control mode (PCCM), which gives the circuit an advantage in a form of natural feed forward control. The outer-loop is de-signed to compensate the difference between the average current and the peak current of inductor L.

$$L = 2l\left(\ln\left(\frac{2l}{d}\left(1+\sqrt{1+\left(\frac{d}{2l}\right)^2}\right)\right) - \sqrt{1+\left(\frac{d}{2l}\right)^2} + \frac{\mu}{4} + \frac{d}{2l}\right) \qquad (11)$$

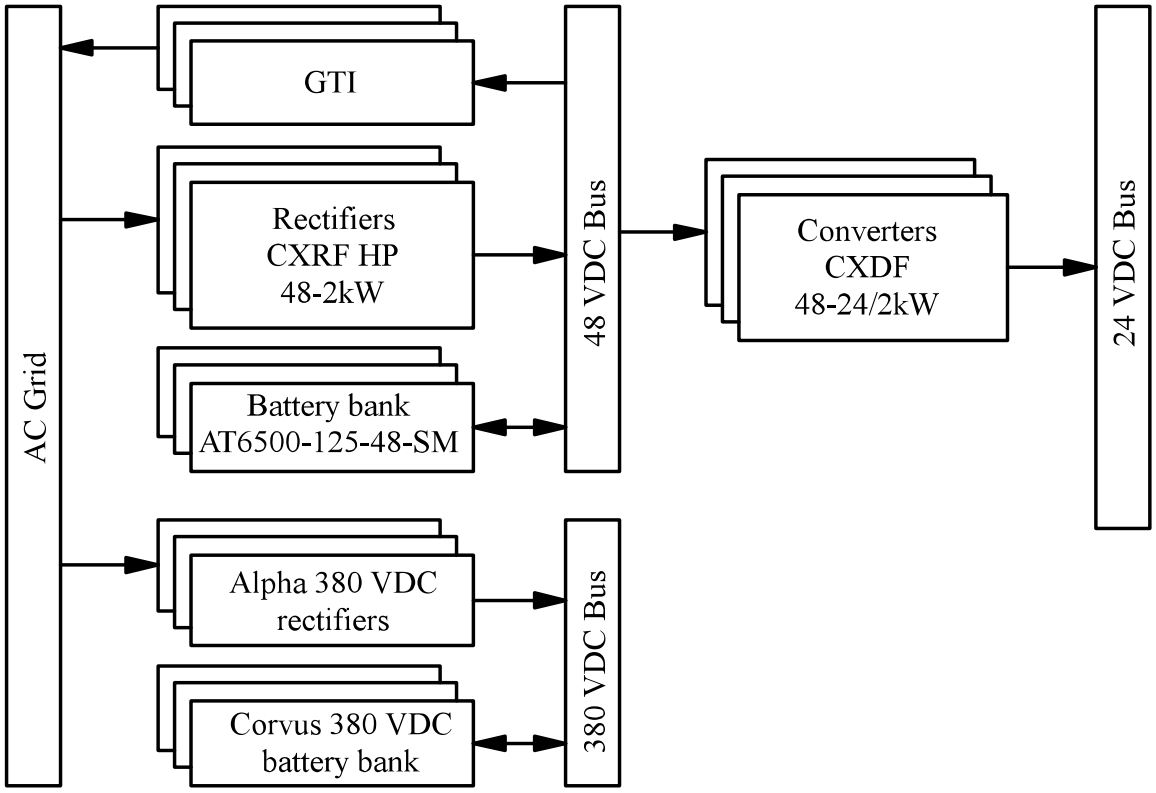


Fig. 5. System diagram of the Alpha AC-DC microgrid in Kaiser building at UBC Electrical and Computer Engineering

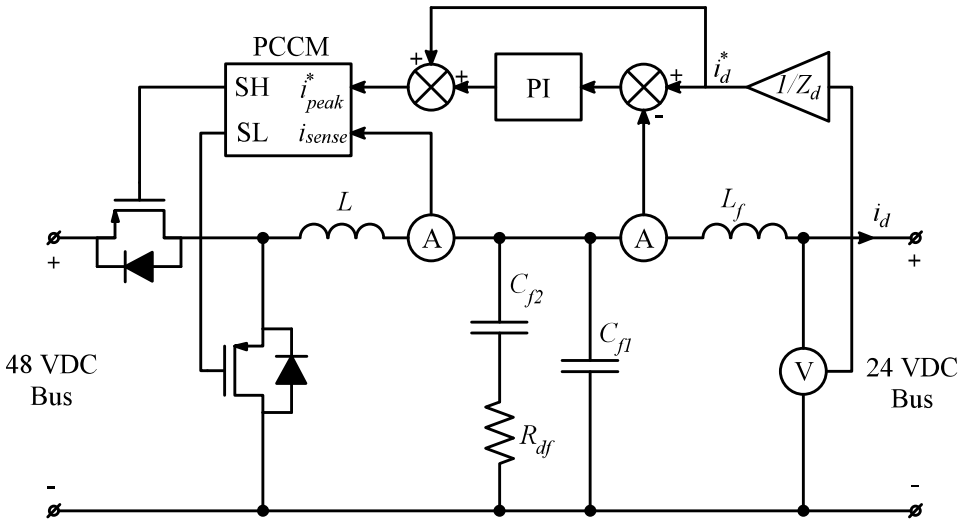


Fig. 6. Auxiliary damper circuit power stage and control diagram

Building Blocks of Simulated Subsystems: The model of the DC subsystem considered in this paper has been implemented in MATLAB/PLECS. The corresponding block-diagram is shown in Fig. 7. The 48 VDC bus integrating the Lithium-ion batteries feeds the 48-to-24 V DC/DC modular converters. The battery model is based on typical state-of-discharge curves with fixed internal resistance. Since the battery has ultra-low impedance, the AC-DC rectifiers of the real system are neglected for the purpose of studies in this paper.

1) 48-to-24 V converter: Each converter is composed of input/output filters and flyback-converter modules operating in discontinuous conduction mode (DCM). An average model of flyback converter based on switching cells was developed to improve the quality and speed of the simulation [27].

2) Cable inductance: A 32 μH parasitic inductance is assumed for a 20-m-length and 10-mm^2-diam cable. Self-inductance for the single cable is calculated using the equation (11) from [28], where d is diameter of the cable, l is total length and μ is absolute magnetic permeability.

3) CPL Model: A finite bandwidth CPL model is considered here. The negative impedance effect is practically limited by the control bandwidth, which can range from tens of Hz to tens of kHz. Therefore, the CPL is considered to possess the negative impedance characteristics up to the frequency where the phase angle starts

rising from □180°. Considering a limited bandwidth, the CPL impedance Z_{in} can be modelled as

$$Z_{in} = -R_l(\tau s + 1), \tag{12}$$

where $\tau = 10^{-4}$ corresponds to the bandwidth of 2 kHz.

Simulation of CPL Plug-in Test: The simulation is performed at 2.5, 5 and 7.5 kW CPL power levels. In addition, a 0.65 kW resistive load was assumed connected on the bus at all times. Three slew rates of 0.37 A/ms, 3.7 A/ms and 37 A/ms are applied separately to the CPL step-change tests. The system without the active damper becomes unstable after the second step-change. The corresponding simulated unstable voltage and power transient waveforms are shown in Fig. 8(a).

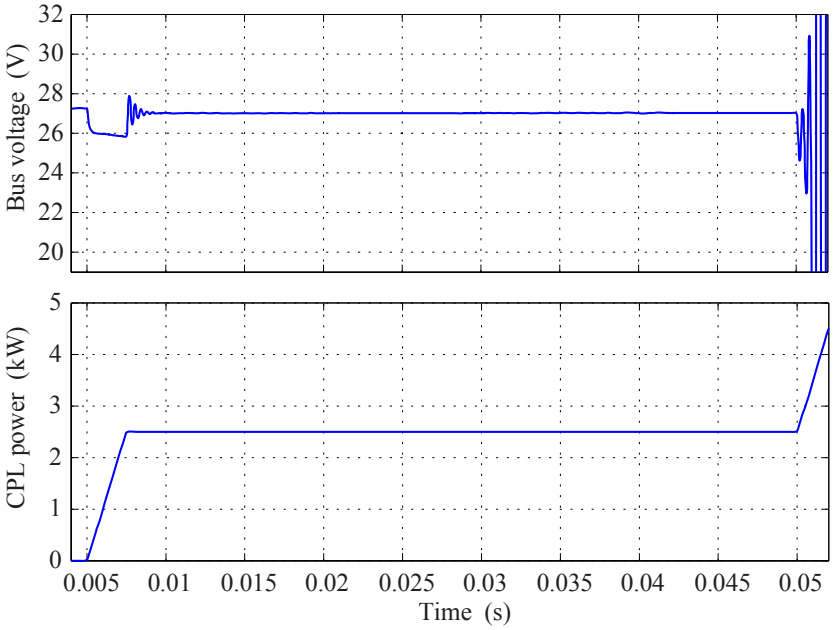
The output impedance of the 24 VDC bus in small-signal sense was extracted from the model using the system analysis tools of MATLAB, and its a 5th order polynomial form is

$$Z_{out}(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \tag{13}$$

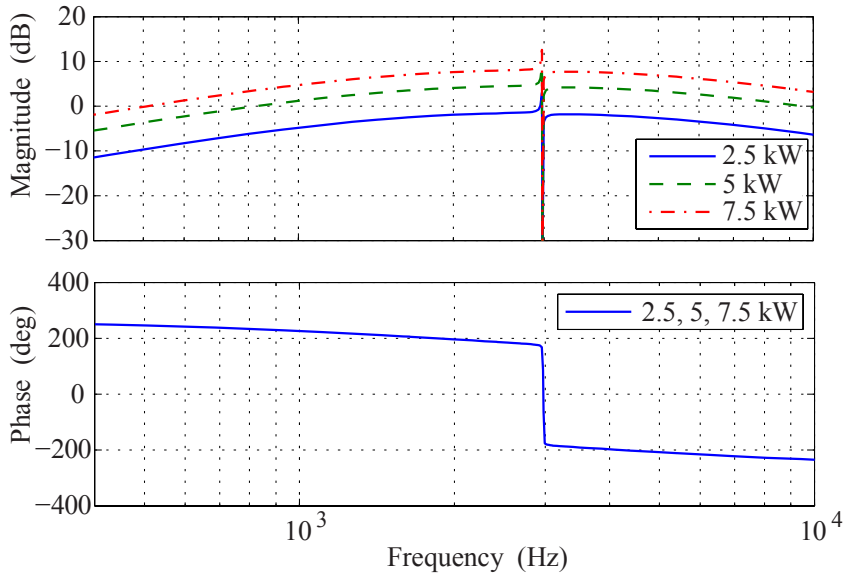
where

$$\begin{cases} a_5 < a_4 < \cdots < a_0 \\ b_5 < b_4 < \cdots < b_0. \end{cases} \tag{14}$$

The small-signal minor loop gain of the above test is shown in Fig. 8(b). Observing from the bode plot, the minor loop gain is under 0 dB at 2.5 kW, which means that the Nyquist criterion is satisfied at this state. However, the Nyquist criterion becomes unsatisfied at higher power levels. This is clearly caused by the CPL phase shift, which brought the system loop gain over the stability margin



(a)



(b)

Fig. 8. 24 VDC bus voltage and current waveforms: (a) voltage and power during CPL step change from 2.5 to 5 kW at the slew rate of 37 A/ms that results in unstable operation; and (b) minor loop gains Z_{out}/Z_{in} of un-damped system

Simulation of Auxiliary Circuit Enabled: To stabilize the system and obtain sufficient stability margins, the minor loop gain Z_{out}/Z_{in} must be reshaped using damping. In this study, we apply the auxiliary circuit to emulate a passive *RC* damper. First, the parameters of the damping circuit can be derived. Assuming that a 10 dB gain margin is required, we can apply the methods introduced above and

derive the set of constraints as follows,

$$\begin{cases} \left| \dfrac{Z_{out}(j\omega) \square Z_d(j\omega)}{[Z_{out}(j\omega) + Z_d(j\omega)] / Z_{in}(j\omega)} \right| = 0.316 \\ CR_l a_5 - CRa_5 + CRR_l b_5 > 0 \\ R_l b_5 - a_5 - CRa_4 + CR_l a_4 + CRR_l b_4 > 0. \end{cases} \tag{15}$$

Using the eigenvalue analysis of the un-damped minor loop gain Z_{out}/Z_{in}, the system oscillation frequency of 2.87 kHz is obtained, which can be also observed from the bode plot of Fig. 8(b). Since the coefficients d_{n-1}, d_{n-2}, …, d_1 of (14) are in an ascending order, only two coefficients, d_6 and d_5, need to be considered. Finally, solving (15), the optimal *RC* parameters are summarized in Table III.

The test with enabled damping circuit is performed under the same conditions as in Section IV-B. The corresponding transients observed at the 24 VDC bus are shown in Fig. 9. As it can observed in Fig. 9, the system is stabilized by the damping circuit with 10 dB gain margin.

To further investigate the effect of active and passive damping, a third test was conducted with load step change from 2.5 to 5 kW at 37 A/ms with passive and active damping applied, respectively. The comparison between two damping circuits is shown in Fig. 10. As it can be seen in Fig. 10, the auxiliary circuit handles the current command current very well and indeed very closely emulates the behavior of a passive *RC* damping circuit. The parameters of the emulated damping circuit are sufficient to stabilize the system. However, the passive *RC* damping circuit will also have additional energy losses. The energy dissipation on the resistor of the passive *RC* damper is

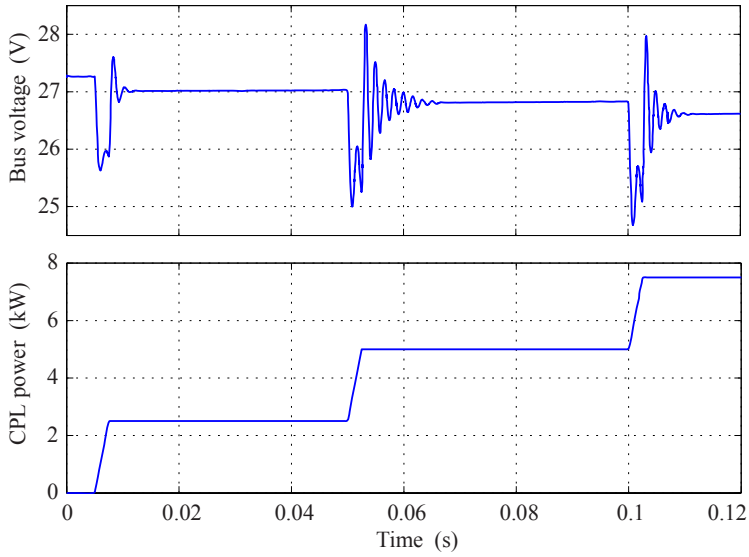
$$E_d = R\int_{t1}^{t2} i_d{}^2 dt \,, \tag{16}$$

where t_1 and t_2 respectively represent the start and end time of one transition period. Based on the results in Fig. 10, the energy dissipation during one damping cycle is 0.028 J, which translates into approximately 0.1 kW power loss when the transient

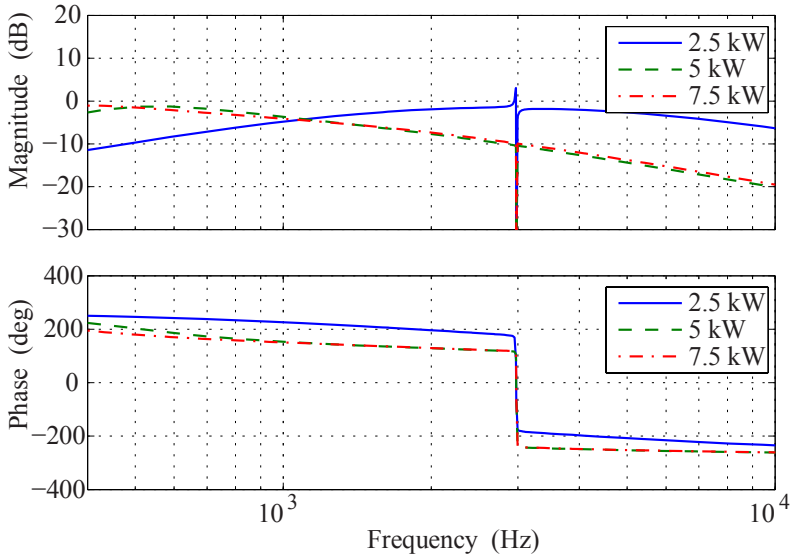
occurs once a second. However, the proposed auxiliary circuit recycles this energy.

TABLE II: CALCULATED DAMPING CIRCUIT PARAMETERS FOR DIFFERENT LOADS

Power level (kW)	5	7.5
R_d (Ω)	0.1	0.07
C_d (μF)	3000	7000



(a)



(b)

Fig. 9. 24 VDC bus voltage and current waveforms depicting stable operation with proposed auxiliary active damping circuit: (a) during CPL step power changes from 2.5 to 5 kW and from 5 to 7.5 kW at the slew rate of 37 A/ms; and (b) minor loop gains Z_{out}/Z_{in} of the damped system

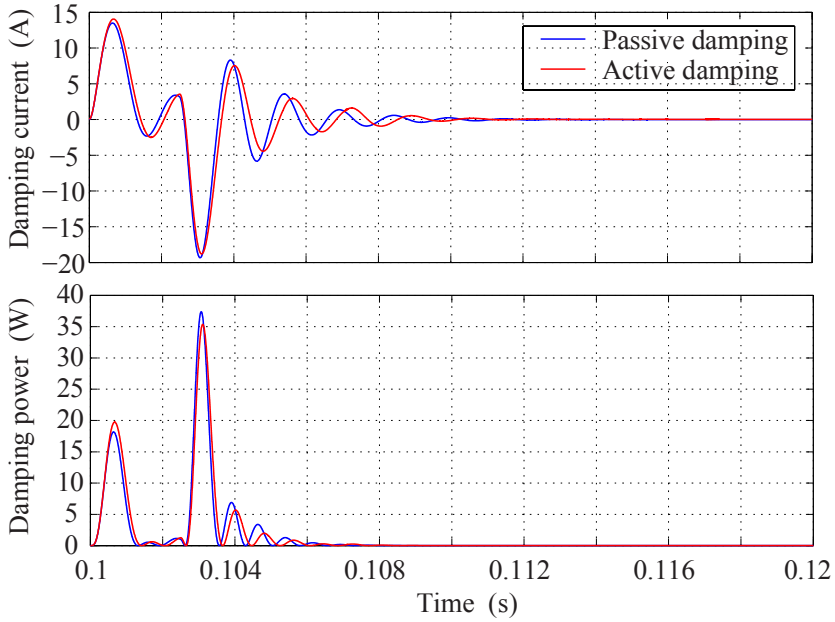


Fig. 10. Damping current from passive *RC* circuit and proposed active auxiliary damping circuit during CPL step change from 5 to 7.5 kW

Conclusions: In this paper, an active damping strategy emulating RC- circuit is introduced to stabilize the DC distribution system feeding CPLs. A hybrid method is proposed to determine the RC-circuit parameters. A bi-directional auxiliary circuit is used to emulate the V-I characteristic of a passive RC damping circuit. The simulation based on MATLAB/PLECS package is performed to verify the proposed active damping strategy. The proposed methodology may lead to a paradigm shift where the smart electronic loads are capable of providing instantaneous power consumptions and impedances to the active damper. According to the source and load information, the auxiliary damper can reconfigure its impedance (and injected current) in real time in order to stabilize the system as the loads are changing, connecting and/or disconnecting. Thus, a robust DC distribution system is achieved.

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