Journal of Nano- and Electronic Physics
Vol. **15** No 1, 01017(5pp) (2023)

Журнал нано- та електронної фізики
Том **15** № 1, 01017(5cc) (2023)

Analysis of Power Supply Voltage Drop (IR-Drop) and Propagation Delay Using Folded Graphene Nano Ribbon Interconnect (F-GNR) Interconnect

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(Received 01 January 2023; revised manuscript received 17 February 2023; published online 24 February 2023)

In this work, a comparative analysis is performed in terms of power supply voltage drop (IR-Drop) and propagation delay (PD) of three different graphene nanoribbon (GNR) based interconnect models i.e., vertical GNR (V-GNR), horizontal GNR (H-GNR), and folded GNR (F-GNR) for next generation high speed and low power IC design. To perform IR-Drop and delay analysis for three different interconnect models, a 10-stage cascaded CMOS inverter (i.e., 16nm PTM-HP CMOS model) is used, where each inverter is connected with three different interconnect models (i.e., V-GNR, H-GNR, and F-GNR). Each interconnect model consists of different RLC values, which are calculated using some standard mathematical model. From the above analysis, it is observed that F-GNR is showing less Peak IR-Drop (~ 200 mV @ 1st stage, ~ 215 @ 5th stage, ~ 232 @ 10th stage) compared with V-GNR (~ 210 mV @ 1st stage, ~ 224.4 @ 5th stage, ~ 256.67 @ 10th stage) and H-GNR (~ 272.33 mV @ 1st stage, ~ 277.88 @ 5th stage, ~ 282.45 @ 10th stage) at 0.4 eV Fermi energy. In terms of power consumption, F-GNR is showing less power consumption (i.e., 2.06e-005 Watt) compared with V-GNR (i.e., 3.80×10^{-5} Watt) and H-GNR (i.e., 4.08×10^{-5} Watt). In terms of propagation delay, F-GNR is showing ~2-5 times less delay in several cascaded stages (i.e., starting from the 1st stage up to the 10th stage) compared with V-GNR and H-GNR interconnect. The above analysis is useful for next-generation high-speed IC design using nano-interconnect materials.

Keywords: Folded Graphene nanoribbon (FGNR), Interconnect, IR-Drop, Delay.

DOI: 10.21272/jnep.15(1).01017 PACS numbers: 81.05.Uw, 63.22.Np, 61.46.Np.

1. INTRODUCTION

Graphene is one of the promising materials for next-generation high-performance integrated circuit design due to its excellent electrical, thermal, and mechanical properties. The structure of graphene is basically a single-layer hexagonal array of carbon atoms arranged in a honeycomb lattice structure [1]. The bandgap of single-layer graphene is zero. A nonzero bandgap is attained when graphene is sliced into a ribbon known as a graphene nanoribbon (GNR). The width of the ribbon has an inverse relationship with the bandgap (E_g). Depending on the width and edge of the ribbon, GNR exhibits metallic or semiconducting properties. Zigzag GNR is a type of GNR that has zigzag edges (ZGNR) and shows always metallic properties, whereas Armchair GNR is a type of GNR with armchair-style edges (AGNR) that shows both metallic and semiconducting properties depending on the width of the GNR. In order for AGNR to be metallic, its width must contain $N = 3k + 2$ (where k is an integer); otherwise, it is semiconducting [2]. Due to its metallic characteristics, the ZGNR is recognized as a novel interconnect material for future interconnect applications. For interconnect modeling, several parallel GNR layers are taken into consideration because of the single-layer GNR's (SLGNR) high quantum resistance. The majority of scientists have modelled MLGNR interconnects with respect to horizontal GNR layers [3-7]. In several research work, the top-contact (TC) or side-contact (SC) MLGNR interconnects are used to investigate the interconnect performance [8-9]. Additionally, it is claimed that despite the SC-MLGNR connection's higher manufacturing burden, it performs better than the TC-MLGNR interconnect [10]. MLGNR interconnects employing vertical GNR (V-GNR) layers have just recently been proposed by a few researchers reported in [11]. Li et. al. revealed that VGNR has greater performance when compared to H-GNR connection after modeling MLGNR interconnect with horizontal and vertical layers [12]. Signal integrity, power consumption and stability analysis are reported in [13]. Here, a comparative study is performed between ML-VGNR interconnect and ML-HGNR interconnect. Two flat GNRs joined by a fractional nanotube can be seen as the basic structure of a folded GNR (F-GNR) [14]. One flat ribbon can be folded to create it. Graphene or GNR is mechanically manipulated to produce folded GNR (F-GNR). Experimental observations of F-GNR have been made by Yu et al., Liu et al., and Zhang et al. [15-17]. The numerical F-GNR interconnect model was first proposed by D. Das et.al. reported in [18-19]. Although numerous researchers have studied GNR for interconnect applications, folded GNR (F-GNR) has never been studied for IR-Drop and propagation delay analysis for nano-electronic circuit applications. In this work, we introduced a folded GNR structure model for interconnect applications.

The rest of the paper is organized as follows. Section 2 represents the interconnect models. Section 3 represents the results and discussion. The conclusions are presented in the Sections 4.

2. INTERCONNECT MODELS

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GNR interconnect is broadly classified as horizontal GNR (H-GNR), vertical GNR (V-GNR) and Folded GNR (F-GNR) (see Fig. 1). Here, H-GNR structure is combination of multiple single layer GNR (SLGNR) also called as multi-layered GNR (MLGNR). A single layer GNR having high quantum resistance $R_Q = (h/2e^2)/N_{ch}$, where h is plank's constant, e is known as charge of electron, and N_{ch} is the total number of conduction channel. The conduction channel is depending on the number of populated sub band (M = Int ($E_F/\Delta E$)), GNR width (W_{GNR}), temperature (T) and Fermi energy (E_F). Here, ΔE is the energy gap between two sub band. Due to high quantum resistance of SLGNR, the H-GNR or MLGNR is preferred for interconnect modeling. H-GNR shows less resistivity due to its parallel configuration and widely used for nano interconnect fabrication. The H-GNR is also classified as two types (a) top-contact (TC-GNR) and (b) side-contact (SC-GNR). The TC-GNR is preferred over SC-GNR due to less manufacturing cost and easy to fabricate. The V-GNR is same as H-GNR but it is represented as vertical structure. Finally, the F-GNR consists only one single layer in a folded form instead of multiple layers. Figure 1 shows the cross-sectional view of H-GNR, V-GNR and F-GNR interconnect. Here, T_h is known as thickness of the interconnect, W is known as interconnect width and H is the height from the ground plane. The number of layers of different GNR structures can be calculated as

$$N = \begin{cases} 1 + Int\left(\frac{T_h}{\delta}\right) & for\ HGNR\left(W_{HGNR} \neq T_h\right) \\ 1 + Int\left(\frac{W}{\delta}\right) & for\ VGNR\ /\ FGNR\left(W_{V,FGNR} = T_h\right) \end{cases}, \quad (1)$$

where, δ is known as interlayer distance which is assumed as 0.34 nm in this work. More GNR layers with the same width as the connector are present in HGNR interconnect structures. VGNR interconnect structures have fewer GNR layers than HGNR structures, but their widths are the same as their connectivity thicknesses.

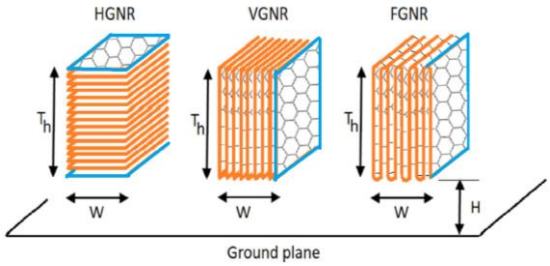

Fig. 1 – Schematic representation of HGNR, VGNR and FGNR interconnect [18-19]

The fundamental N-fold structure of the FGNR interconnect model is depicted in Figure 2. The curved part's length is $\Omega = \pi\delta/2$. The width of N-fold GNR can be represented as

$$W_{FGNR} = (N-1)\Omega + (T_h - \delta)N + \delta \quad (2)$$

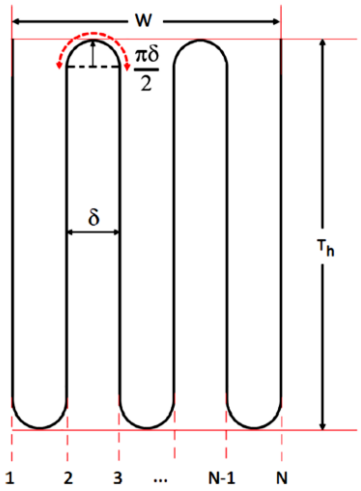

Fig. 2 – Schematic representation of FGNR interconnect [18-19]

Table 1 – Number of GNR layers (N) and width of GNR (WGNR) layer for different GNR structures and different technology nodes

Technology (nm)	16	22
N for HGNR	95	130
N for VGNR	48	65
N for FGNR	1	1
WHGNR (nm)	16	22
WVGNR (nm)	32	44
WFGNR (nm)	1545	2872

The number of GNR layer (N) and width (W) of three different types of interconnects can be measure using equation (1) and (2). Table 1 represents the number of layer and width calculated data for two different technology (i.e., 16 nm and 22 nm). In this work, we mainly considered the 16 nm technology. The resistance model of single layer GNR is represented as

$$R_{SLGNR} = R_Q \left[\sum_{n=1}^{M} N_{ch,n}\left(1 + \frac{L}{\lambda}\right)^{-1}\right]^{-1}, \quad (3)$$

here, R_Q is represented as quantum resistance, $N_{ch,n}$ is known as number of conduction channel in each single layer GNR, L is the interconnect length and λ is represented as mean free path (MFP). There are N number of parallel SLGNR layers in a multilayer GNR (MLGNR) configuration. As a result, the formula for the resistance of the L-length MLGNR structure is

$$R_{MLGNR} = R_{SLGNR} / N \quad (4)$$

The per unit length kinetic inductance of MLGNR is expressed as

$$L_{K,MLGNR} = L_K / N_{ch,n}N, \quad (5)$$

where $L_K = h/(4e^2 v_F) = 6.5$ nH/μm and v_F is the Fermi velocity in graphene which is 1×10^6 m/s.

The per unit length quantum capacitance of MLGNR is expressed as

$$C_{Q,MLGNR} = C_Q / N_{ch,n}N, \quad (6)$$

where $C_Q = 4e^2/(hv_F) = 154.54$ aF/μm.

3. RESULTS AND DISCUSSION

In this section, we will discuss the power supply voltage drop (IR-Drop), delay, and power consumption estimation of a 10-stage cascaded CMOS inverter circuit (see Fig. 3). In each stage two CMOS inverter is connected back-to-back using interconnect. The interconnect is nothing but a combination of RLC structure. Here, mainly three different GNR based interconnect structure is used (i.e., VGNR, HGNR, and FGNR) for performance analysis. The entire analysis is performed using 16 nm PTM-HP CMOS model and 16 nm interconnect model (i.e., three different interconnect structures VGNR, HGNR and FGNR). The TSPICE (Tanner-EDA) and MATLAB simulation tool are used for circuit simulation and analysis. To calculate IR-Drop, delay, and power consumption in each stage, the resistance value for all three types of interconnects plays an important role. In this analysis, we calculated the resistance values for HGNR, VGNR, and FGNR for different interconnect lengths (10 μm to 100 μm) and four different Fermi potentials (0.1 to 0.4) (see Table 2 to Table 5), After that, we replaced the value in the real circuit to check the performance in terms of delay and IR-Drop of three different interconnect structure. In this analysis, supply voltage (V_{DD}) is considered as 0.7 V and a rising pulse is applied at the input of the 1st inverter. The width of the pulse is considered as 20 ns and the period of the pulse is considered as 40 ns. Pulse rise and fall time is considered as 1 ns.

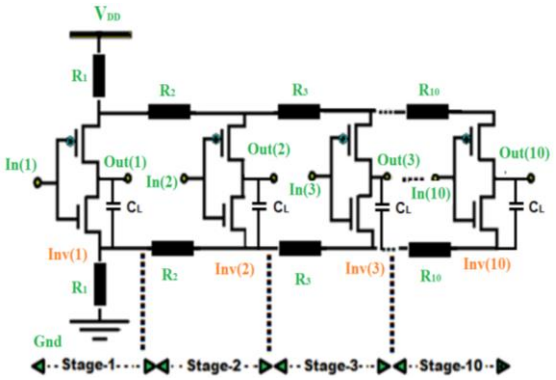

Fig. 3 – Schematic representation of 10-stage cascaded CMOS inverter circuit with three different interconnect materials

Table 2 – Resistance of HGNR, VGNR, FGNR Interconnect at different interconnect length @ $E_F = 0.1$

At $E_F = 0.1$ Length (μm)	HGNR R (kΩ)	VGNR R (kΩ)	FGNR R (kΩ)
10	77.23	51.25	35.55
20	154.46	102.5	71.1
30	231.69	153.75	106.65
40	308.92	205	142.2
50	386.15	256.25	177.75
60	463.38	307.5	213.3
70	540.61	358.75	248.85
80	617.84	410	284.4
90	695.07	461.25	319.95
100	772.3	512.5	355.5

Table 3 – Resistance of HGNR, VGNR, FGNR Interconnect at different interconnect length @ $E_F = 0.2$

At $E_F = 0.2$ Length (μm)	HGNR R (kΩ)	VGNR R (kΩ)	FGNR R (kΩ)
10	56.66	44.14	31.22
20	113.32	88.28	62.44
30	169.98	132.42	93.66
40	226.64	176.56	124.88
50	283.3	220.7	156.1
60	339.96	264.84	187.32
70	396.62	308.98	218.54
80	453.28	353.12	249.76
90	509.94	397.26	280.98
100	566.6	441.4	312.2

Table 4 – Resistance of HGNR, VGNR, FGNR Interconnect at different interconnect length @ $E_F = 0.3$

At $E_F = 0.3$ Length (μm)	HGNR R (kΩ)	VGNR R (kΩ)	FGNR R (kΩ)
10	46.77	38.54	24.11
20	93.54	77.08	48.22
30	140.31	115.62	72.33
40	187.08	154.16	96.44
50	233.85	192.7	120.55
60	280.62	231.24	144.66
70	327.39	269.78	168.77
80	374.16	308.32	192.88
90	420.93	346.86	216.99
100	467.7	385.4	241.1

Table 5 – Resistance of HGNR, VGNR, FGNR Interconnect at different interconnect length @ $E_F = 0.4$

At $E_F = 0.4$ Length (μm)	HGNR R (kΩ)	VGNR R (kΩ)	FGNR R (kΩ)
10	43.4	35.2	21.1
20	86.8	70.4	42.2
30	130.2	105.6	63.3
40	173.6	140.8	84.4
50	217	176	105.5
60	260.4	211.2	126.6
70	303.8	246.4	147.7
80	347.2	281.6	168.8
90	390.6	316.8	189.9
100	434	352	211

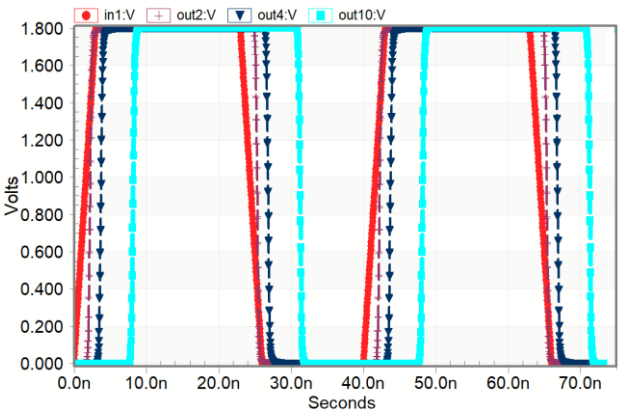

Fig. 4 – Input and output waveform 10-stage CMOS inverter

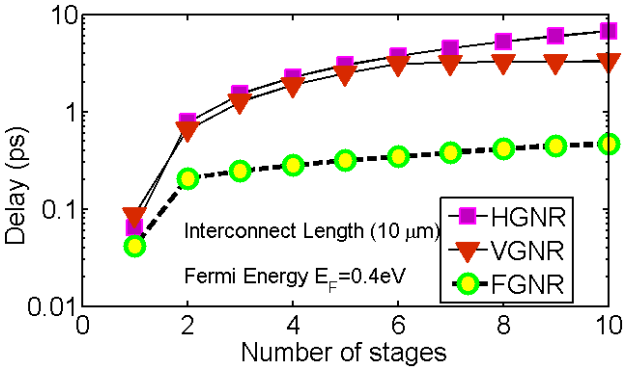

Fig. 5 – Delay vs. number of stages CMOS inverter

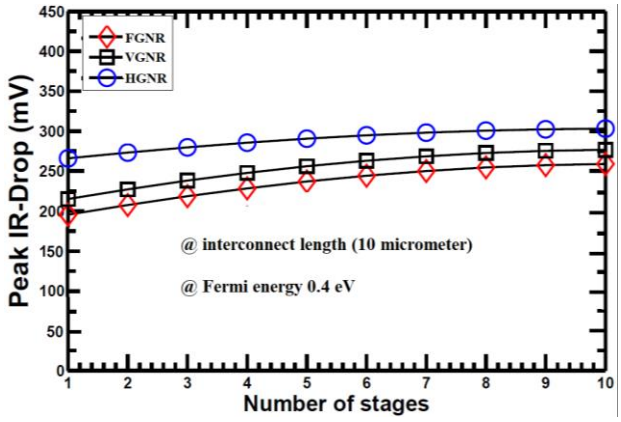

Fig. 6 – Peak IR-Drop vs. number of stages CMOS inverter

Table 3 – Power calculation of HGNR, VGNR, FGNR Interconnect @ 10 μm interconnect length, @E_F = 0.4

At E_F = 0.4 and length 10 μm	Power consumption in watts		
No of stages	HGNR	VGNR	FGNR
Max Power	6.90×10^{-5}	5.89×10^{-5}	3.01×10^{-5}
Min Power	2.71×10^{-5}	1.71×10^{-5}	1.05×10^{-5}
Average Power	4.08×10^{-5}	3.80×10^{-5}	2.06×10^{-5}

Fig. 4 shows the transient response of 10-stage cascaded inverter circuit using TSPICE simulation tools. Here, red color represents the input wave form and other colors are the output response of consecutive stages. When input signal is propagating from one stage to another stage through interconnect it is producing delay due to RC time constant, which represented as $\tau_P = R \cdot C$. As the number of stages and interconnect length will increase, it will produce more delay. From Fig. 5 it is observed that FGNR is the best MLGNR structure because it is showing less delay ~ 2-5 × less compared with VGNR and HGNR interconnect at 10 μm interconnect length when Fermi energy is 0.4 eV. In terms of IR-Drop, it is observed that F-GNR is showing less Peak IR-Drop (~ 200 mV @ 1st stage, ~ 215 @ 5th stage, ~ 232 @ 10th stage) compared with V-GNR (~ 210 mV @ 1st stage, ~ 224.4 @ 5th stage, ~ 256.67 @ 10th stage) and H-GNR (~ 272.33 mV @ 1st stage, ~ 277.88 @ 5th stage, ~ 282.45 @ 10th stage) at 0.4 eV Fermi energy. In terms of power consumption, F-GNR is showing less power consumption (i.e., 2.06×10^{-5} Watt) compared with V-GNR (i.e., 3.80×10^{-5} Watt) and H-GNR (i.e., 4.08×10^{-5} Watt). In terms of propagation delay, F-GNR is showing ~ 2-5 times less delay in several cascaded stages (i.e., starting from the 1st stage up to the 10th stage) compared with V-GNR and H-GNR interconnect. In all aspect FGNR is showing better performance compared with HGNR and VGNR.

4. CONCLUSION

In this work, we analyzed the performance of three different GNR interconnect models. A comparative analysis is performed in terms of power supply voltage drop (IR) drop, propagation delay $\tau_P = R \cdot C$, and power consumption. From the above analysis it is observed that FGNR is superior GNR structure compared with HGNR and VGNR for next generation nano interconnect modeling due to its less resistivity. As a result, propagation delay, IR-Drop and power consumption will be less in FGNR model compare with VGNR and HGNR. The above analysis highlights the is useful ness of FGNR interconnect structure for next-generation high-speed IC design.

ACKNOWLEDGEMENT

This work is partially supported by SR University, Warangal, Telangana, India.

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Аналіз падіння напруги джерела живлення (IR-Drop) і затримки поширення з використанням з'єднань зі складеною графеновою нанострічкою (F-GNR)

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У даній роботі виконано порівняльний аналіз з точки зору падіння напруги джерела живлення (IR-Drop) і затримки поширення (PD) трьох різних моделей з'єднання на основі графенових нанострічок (GNR), тобто вертикального GNR (V-GNR), горизонтального GNR (H-GNR) і складений GNR (F-GNR) для високошвидкісної та малопотужної конструкції IC нового покоління. Для виконання ІЧ-відпаду та аналізу затримки для трьох різних моделей з'єднань використовується 10-ступінчастий каскадний КМОП-інвертор (тобто 16-нм модель PTM-HP CMOS), де кожен інвертор з'єднаний із трьома різними моделями (тобто V-GNR, H-GNR і F-GNR). Кожна модель з'єднання складається з різних значень RLC, які обчислюються за допомогою стандартної математичної моделі. З наведеного вище аналізу видно, що F-GNR демонструє менше пікового ІЧ-спаду (~ 200 мВ на 1-му етапі, ~ 215 на 5-му етапі, ~ 232 на 10-му етапі) порівняно з V-GNR (~ 210 мВ на 1-му етапі). стадія, ~ 224,4 на 5-й стадії, ~ 256,67 на 10-й стадії) і H-GNR (~ 272,33 мВ на 1-й стадії, ~ 277,88 на 5-й стадії, ~ 282,45 на 10-й стадії) при 0,4 еВ енергії Фермі. Стосовно енергоспоживання, F-GNR демонструє менше споживання енергії (тобто $2{,}06{\cdot}10^{-5}$ Вт) порівняно з V-GNR (тобто 3.80×10^{-5} Вт) і H-GNR (тобто 4.08×10^{-5} Вт). З точки зору затримки розповсюдження, F-GNR демонструє приблизно в 2-5 разів меншу затримку на кількох каскадних етапах (тобто, починаючи з 1-го етапу до 10-го етапу) у порівнянні з V-GNR і H-GNR з'єднанням. Наведений вище аналіз корисний для проектування високошвидкісних IC наступного покоління з використанням матеріалів нанозв'язку.

Ключові слова: Складена графенова нанострічка (FGNR), Міжелементне з'єднання, IR-відсіч, Затримка.