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INVESTIGATION OF CARRIER MOBILITY DEGRADATION EFFECTS ON MOSFET LEAKAGE SIMULATIONS

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Abstract: The term *carrier mobility* generally alludes to both electron and hole mobility in semiconductors. These parameters characterize how quickly an electron and/or hole moves through a metal or semiconductor when under the influence of an electric field. Most studied mobility models only take into account the influence of temperature and doping concentration which provides less accurate but faster simulation and allows preliminary device description adjustments and analysis. However complete models, like Klaassen, Shirahata or some allowed model combination give results that better fit experimental curves. This work focuses on such possibilities and shows that, as carriers are accelerated in an electric field, their velocity will begin to saturate when the electric field magnitude becomes significant. Such effects are observed in low, high and inversion mobility models simulated in strain-Silicon devices. These effects are to be accounted for by reducing of the effective mobility. Furthermore, it is shown that charge carriers in semiconductors are electrons and holes and that, their numbers are controlled by the concentrations of impurity elements, i.e. doping concentration; for that reason doping concentration has great influence on carrier mobility. Carriers are able to flow more quickly in materials with higher mobility; since the speed of an embedded device is limited by the time it takes a carrier to move from one side to the other. Devices composed of materials with higher mobility are able to achieve higher speeds. *Copyright © Research Institute for Intelligent Computer Systems, 2016. All rights reserved.*

Keywords: electron mobility, transconductance, strain silicon, hole mobility, semiconductor, transistor, leakage, simulation.

1. INTRODUCTION

In solid-state physics, the electron mobility describes how fast electrons move through a metal or semiconductor, in the presence of an electric field. An analogous quantity exist for holes in semiconductors technologies and is known as hole mobility. The term carrier mobility therefore refers in general to both electron and hole mobility in semiconductors. Carrier mobility models fall into one of four categories namely: numerical, physical, semi-empirical, and empirical. Physical mobility models result from first principle calculations; i.e. critical components such as coefficients and power dependencies present in the model are obtained from fundamental calculations. In practice, physical mobility models seldom agree with experimental values since a considerable amount of assumptions and simplifications are made in order to arrive at the final solution. Therefore, to reconcile the model with experimental data, the coefficients appearing in the physical mobility model are allowed to vary from their original values. In this process the power-law dependencies resulting from the first-principles calculation are preserved, and the resulting model is termed semi-empirical.

At the other end of the spectrum are empirically-based models in which the power-law dependencies are also allowed to vary. In [28] it is shown that empirical models have much lesser physical content when compared to the other two models, and also display a much restricted range of validity. Empirical models are usually used when the dependencies predicted by the first principle calculations don't permit a good fit between the

experimental data and the analogous semi-empirical model [28].

Carrier mobility is a special case of electrical mobility of charged particles in a fluid under an applied electric field [29]. When an electric field is applied across a piece of material, electrons respond by moving with an average velocity called the drift velocity. In a study conducted by [2], researchers found that mobility is proportional to the relaxation time of the electrons and inversely proportional to their effective mass. They showed that the drift velocity of electrons in an electric field can be approximated by the following equation:

$$v_n = -\frac{q\tau_n}{m_e^*}\varepsilon = \mu_n\varepsilon \quad (1)$$

In (1), q represents the electrons charge, τ_n is the relaxation time of electrons. The quantity m_e^* represents the effective mass of electrons while μ_n is the electron mobility; v_n is the average drift velocity and ε is the electric field. From (1), the electron mobility μ_n can be expressed as:

$$\mu_n = -\frac{v_n}{\varepsilon} = \frac{q\tau_n}{m_e^*} \quad (2)$$

Since mobility is proportional to the relaxation time, it decreases with temperature increase because thermal lattice vibrations increase with temperature. Likewise, defect and impurities accentuate electron collisions and so mobility decreases with increasing impurity and defect concentration. Conductivity is a function of the product of the carrier concentration and mobility. For instance, the same conductivity could be measured for a tiny number of electrons with high mobility or a huge number of electrons with a small mobility [29]. A similar behavior is not observed in the case of metals since most metal electrical behavior depends on its conductivity alone. Therefore mobility is relatively unimportant in metal physics [29].

On the other hand, for semiconductors, the behavior of transistors and other devices is dependent on whether there are many electrons with low mobility or few electrons with high mobility. Therefore mobility is a key parameter for semiconductor materials. Almost always, higher mobility translates to better device performance, with other variables equal. However, as MOSFET continue to shrink in size; both the dopant impurities and the fields in the channel will keep rising. All those changes decrease the carrier mobility, and hence the device's transconductance. The transconductance of the MOSFET has a direct effect on its gain and is proportional to the hole or electron mobility (depending on device type); at least for low drain voltages. The transverse field dependent mobility models are of particular importance for simulating MOS devices. Because the reduction of channel lengths in CMOS devices is not accompanied by a corresponding reduction in drain voltage, it causes the electric field in the channel to rise. This results in both velocity saturation of the carriers as well as limiting the current and the transconductance. The reduction in carrier mobility is a major cause of drain current degradation which in turn further reduces the speed of the device.

To enhance the mobility in the inversion layer of MOSFETs, strained silicon (strained-Si) is regarded as possible alternatives to conventional Si devices mostly for deep submicron devices [3]. Strained-Si is a technology that entails stretching or compressing the silicon crystal lattice through various techniques, which in turn increases carrier mobility and enhances the performance of the transistors without having to reduce their physical structures. There are several numerical mobility models reported in the literature. In this work an investigation of the effect of carrier mobility (low, high and inversion), carrier concentrations, transconductance, and electron velocity in strained-Si devices is carried out to optimize CMOS transistor design to produce results that can better fit the experimental curves. Elastic scattering processes including acoustic phonon scattering, neutral impurity scattering and ionized impurity scattering are considered and their relationship to temperature and doping concentration are discussed.

2. MOBILITY MODELLING

Electrons and holes get accelerated in the presence of an electric field. However, they lose momentum due to collisions or scattering with impurities. Scattering is caused by the presence of lattice vibrations (phonons), impurity ions, other carriers, surfaces and other material imperfections. Considering that the effects of all of these microscopic phenomena are grouped into the macroscopic mobilities introduced by the transport equations, these mobilities are proportional to the local electric field, lattice temperature, doping concentration, and so on. Mobility modelling is normally divided into:

1. Low-field mobility,
2. High field mobility,
3. Inversion mobility.

2.1 INVERSION MOBILITY

Experimental evidences indicate that the inversion mobility layer when investigated as a function of the electric field component normal to the S_i/S_iO_2 interface is a function of the doping concentration, the gate and substrate bias and the

oxide thickness. The effective mobility is a spatial average of the mobility profile in the inversion layer. In [1] it was demonstrated that if the effective mobility of electrons is plotted as a function of the effective transverse electric field in the inversion layer, the universal mobility curve is obtained.

The effective field (E_{eff}) of electrons in the inversion mobility layer is computed as the average of the normal electric field $E_y(y)$ experienced by the electrons weighted by the electron concentration $n_y(y)$.

$$E_{eff} = \frac{\int_0^{y_i} E_y(y)n(y)dy}{\int_0^{y_i} n(y)dy} \tag{3}$$

The integration in (3) is performed over the depth of the inversion layer, y_i. When rewritten as a function of the field at the top (E_{top}) and bottom (E_{bottom}) of the inversion layer, the effective field in (3) becomes

$$E_{eff} = \frac{E_{top} + E_{bottom}}{2} = \frac{1}{\varepsilon_{si}}\left(\frac{Q_{inv}}{2} + Q_{depl}\right) \tag{4}$$

Where $E_{top} = \frac{Q_{inv} + Q_{depl}}{\varepsilon_{si}}$ and $E_{bottom} = \frac{Q_{depl}}{\varepsilon_{si}}$

Q_{inv} and Q_{depl} denote the inversion and depletion charge densities, respectively, and can be computed as:

$$Q_{inv} = -q\int_0^{y_i} n(y)dy$$

$$Q_{depl} = \sqrt{(4\kappa_{si}\phi_B N_{sub})/q}$$

The definition of E_{eff} in (4) is valid for electrons on oriented surfaces and can be generalized as:

$$E_{eff} = \frac{1}{\varepsilon}\left(\eta Q_{inv} + Q_{depl}\right) \tag{5}$$

The parameter η is dependent on the orientation of the crystal surface and can assume values different from 1/2 due to valley re-population effects. For estimating the electron mobilities on oriented surfaces, $\eta \approx \frac{1}{3}$ can be assumed.

2.2 HIGH FIELD MOBILITY

When an applied lateral field is increased, electrons and holes gain energies above the ambient thermal energy. At that point in time they are capable of transferring energy to the lattice by optical phonon emission. Such effect induces a saturation of the carrier velocity. To account for this velocity saturation, the mobility has to be reduced accordingly. Popular models that take into consideration this basic feature include the Caughey and Thomas expression [4]

$$\mu = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 E}{v_s}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{6}$$

Modifications to (6) by authors of [5] is as follows:

$$\mu_E = \frac{2\mu_0}{1 + \left[1 + \left(\frac{2\mu_0 E}{v_s}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{7}$$

Where μ_0 denotes the low field mobility and v_s the saturation velocity. The parameter β influences the transition from low to high fields. Equations (6) and (7) are not just applicable to uniform fields; they can also be used for device simulations where the fields are non-uniform. However an appropriate choice of the lateral field must be made. It is worth mentioning at this stage that although (7) describes the high field behavior in unstrained Si, it cannot produce the characteristics of the velocity field relation in the strained case. Equation (8) has been suggested which handles all types of velocity-field characteristics resulting from the Monte Carlo simulations as performed in [5]:

$$v_E = \frac{2\mu_{EE}E}{1 + \left[1 + \left(\frac{2\mu_{EE}E}{v_s(1-\xi)}\right)^{\beta}\right]^{\frac{1}{\beta}}} + v_s\xi\frac{\left(\frac{E}{\eta}\right)^{\gamma}}{1 + \left(\frac{E}{\eta}\right)^{\gamma}} \tag{8}$$

Where μ_{EE} denotes the low-field mobility in the field direction, obtained by projection of the low-field mobility tensor as:

$$\mu_{EE} = e_E^T \cdot \mu_0 \cdot e_E \tag{9}$$

The relevance of the parameter ξ is twofold: (1) it caters for the velocity plateau occurring approximately at $v_s(1-\xi)$ and (2) it also caters for the small negative differential mobility occurring in strained-Sifor higher strain levels. Parameters η and γ are defined as fitting parameters.

2.3 LOW FIELD INVERSION MOBILITY

The low-field mobility is modelled by an expression similar to that proposed by [4].

$$\mu_{LI} = \mu_{min} + \frac{\mu_L - \mu_{min}}{1 + \left(\frac{C_1}{C_{ref}}\right)^{\gamma}} \tag{10}$$

Where C_1 denotes the concentration of ionized impurities, μ_L is the mobility in undoped material,

μ_{min} is the mobility in highly doped material, limited by impurity scattering. The maximum μ_L mobility and minimum μ_{min} mobility, and the parameters describing the mobility decrease with rising impurity concentration. Also C_{ref} and γ are calibrated against an extensive analysis of available simulations results and experimental data.

3. REVIEW OF PREVIOUS WORK

Recently, strained-Silicon technology has been explored abundantly in an effort to increase CMOS based device performance [6-10]. The mobility advantage the strain offers at no significant additional processing cost makes it an ideal candidate among conventional Silicon devices for performance enhancement. Although much work has been conducted on strained-Si structure for mobility enhancement in the inversion layer of MOSFETs, not much has been done in analyzing carrier mobility degradation effects on MOSFET structures.

In the work conducted by researchers of [11] mobility is modelled for strained-Si MOSFETs accounting for various scattering mechanisms such as surface roughness scattering, phonon scattering and coulomb scattering. The authors proposed a strained-Si n-type based Monte Carlo simulator by adapting a previous unstrained-Si; one which includes inversion-layer quantization and a non-parabolic band model. In their research, a new electron mobility model for strained-Si MOSFETs is developed. The increase in mobilityproduced by the strain in the silicon layer is studied and described by means of simple analytical expressions. The authors show that their model can be included in conventional device and circuit simulators. The need for a surface-roughness model dependent on the germanium mole fraction is also highlighted. The developed model agrees pretty well with experimental measurements. The authors however make no mention on the performance of the model under various mobility models.

Authors of [12] developed an electron and hole mobility analytical model for strained-Si MOSFETs. The mobility enhancement for both electrons and holes in strained-Si layer is studied by analytical expressions only. No forms of simulations are carried out to validate their results. In their research, a new electron and hole mobility analytical model for strained-Si MOSFETs is developed. The mobility enhancement in the strained-Si layer is studied and described by means of simple analytical expressions. The dependence of mobility on strained-Si layer thickness in the model is highlighted.

A more in depth study was carried out by the authors of [13]. In their paper, a charge sheet surface potential based model for strained-Si n-MOSFETs is presented and validated with numerical simulation. The model considers sub-band splitting in the 2-DEG at the top hetero-interface in SiGe layer and also the dependence of electron concentration at hetero-interface with the gate oxide. The model is scalable with strained-Si material parameters with physically derived flat-band voltages. An explicit relation for surface potential as a function of terminal voltages is developed. The model is derived from regional charge-based approach, where regional solutions are physically derived. The model gives an accurate description of drain current both in the weak and strong inversion regions of operation. The results obtained from the model developed are benchmarked with commercial numerical device simulator and is found to be in excellent agreement.

With conventional Silicon MOSFETs being scaled down through to nanometre dimensions, maintaining performance enhancement beyond the 22-nm technology node is becoming very difficult. A combination of strain and stress engineering has now become extremely useful to meet the performance targets set by the International Technology Roadmap for Semiconductors (ITRS) [14]. According to the ITRS roadmap, a highly controlled process flow for the incorporation of new material such as, strained-Si in Silicon CMOS technology is becoming crucial for deep sub-micron CMOS devices [15]. Among the viable alternatives, engineered substrates, in particular, substrate-induced strained silicon (strained-Si) seems to be highly promising options for channel engineered MOSFETs as it has been shown to improve CMOS performance [16-20].

4. THE STRAINED SILICON TECHNOLOGY

The transistor performance can be improved in three major ways: (i) increasing the CMOS gate capacitance C_{oxide}, (ii) improving the carrier mobility (μ), or (iii) decreasing the channel length (L).

All of these methods increase the transistor drive current, which in turn improves the device's speed. In this research however, the second option is investigated through strained silicon technology.

Strained-Si technology for improving CMOS based transistor performance appears to be the closest to commercialization. It has been reported that both IBM and Intel are working with semiconductor fabrication facilities to incorporate this technique into their processes. A schematic diagram of a strained-Si n-MOSFET is shown in Fig. 1.

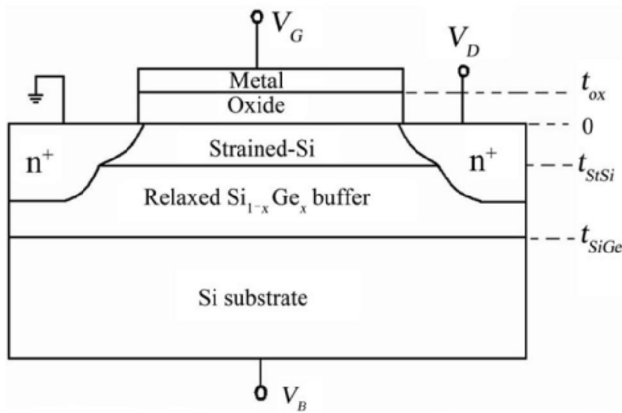

Fig. 1 – Strained Silicon architecture

Here V_G, V_D and V_B represent the gate, drain, and bulk voltages, respectively. It may be noted that for the n-MOSFET, V_G and V_D are positive voltages while V_B is usually negative. The device consists of an SiO_2 gate dielectric layer of thickness t_{ox}, and strained-Si layer of thickness t_{SiSi}, and a relaxed SiGe buffer layer of thickness t_{SiGe}. These layers are grown on a p-type substrate.

Transistors manufactured with strained-silicon wafers have shown far greater charge-carrier mobility than those using conventional substrates. Also the drive current (also known as the output current) of the CMOS devices has also significantly improved. Drive current is a function of the carrier mobility, but also depends on other factors such as the device geometry and its capacitance. A larger drive current boosts the switching speed of the transistor, so that circuits run at higher clock rates. In strained-Si, germanium atoms replace some of the silicon atoms near the wafer's crystalline surface; a thin layer of silicon is then grown on top of the SiGelayer. Because germanium atoms are larger than silicon atoms, the distance between the atoms in the silicon-germanium layer is larger than it is in pure silicon. So when the top silicon layer is grown, its atoms line up with the silicon-germanium below, and it becomes strained (stretched) in the two directions parallel to the plane of the wafer and compressed in the perpendicular direction as shown in Fig. 2. It is in this top strained-silicon layer that the transistors are fabricated.

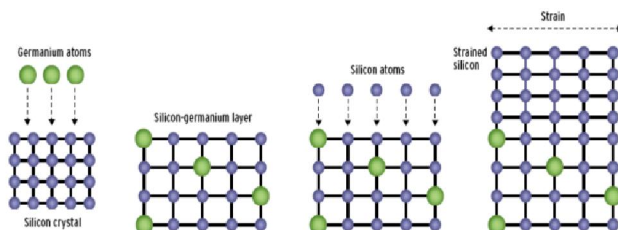

Fig. 2 – Strained-Si steps

5. DESIGN SIMULATION OF STRAINED SILICON N-CHANNEL MOSFET

In this paragraph, the design flow of the structure of strained silicon n-channel MOSFET is discussed in details. The strained-Si MOSFET is fabricated virtually in TCAD tools as described in [21]. Process simulation for the virtual fabrication as well as device simulation is done in ATLAS for characterization of the transistor in the following 4 runs:

1. Definition of an optimum grid using a variable for surface mesh spacing.
2. Selection and inclusion of the selected Mobility Models.
3. Running of the I_d/V_{gs} simulation at low V_{gs}.
4. Overlaying of I_d/V_{gs} curves and mobility in Tonyplot.

The grid generation and structure definition part of the input file follows a default standard syntax as outlined in [22]. Finer grid spacing is important in resolving the high electric field and carrier concentration gradients at the surface.

According to [22] the key areas for a tight mesh when simulating CMOS device are:

1. Very small vertical mesh spacing in the channel below the gate. The exact size of mesh required depends on the transverse field or surface mobility model chosen.
2. Lateral mesh spacing along the length of the channel for deep sub-micron devices. This is required to get the correct source-drain resistance and to resolve the channel pinch-off point.
3. Lateral mesh at the drain/channel junction for breakdown simulations. This is required to resolve the peak of electric field, carrier temperature and impact ionization.
4. Several vertical grid spacing inside the gate oxide when simulating gate field effects such as gate induced drain leakage (GIDL) or using any hot electron or tunneling gate current models.

The fabricated structure created consists of the following parameters:

Type of MOSFET: uniaxial strained silicon PMOS

Oxide thickness = 4.5nm

Gate length = 100nm

Thickness of strained silicon layer = 4.5nm

Germanium fraction used in Si1-xGex, x = 0.35

As stated earlier, the four models analyzed in this work are the Lombardi CVT, Klaassen, Yamaguchi and Modified Watt.

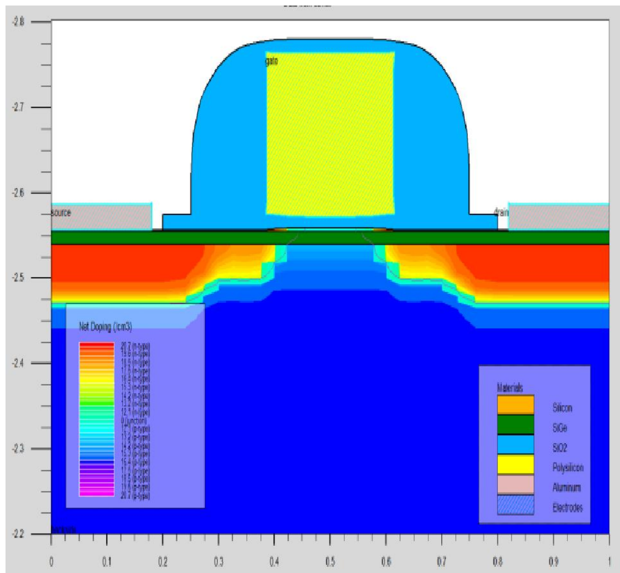

Fig. 3 – Fabricated Model

6. RESULTS

The electrical characteristics of the fabricated device were simulated in ATLAS, a Silvaco modelling and simulation tool. Unlike other modelling software packages, Silvaco uses physics-based simulation rather than empirical modelling. Although empirical modelling produces reliable formulas that match existing data, physics-based simulations however predict the device's performance based upon physical structure and bias conditions. Atlas graphically represents a device on a two-dimensional grid with designated electronic meshing parameters as shown in Fig. 3. At every mesh intersection, the program simulates carrier transport by means of differential equations derived from Maxwell's laws.

6.1. DEVICE I-V CHARACTERISTICS

The threshold voltage is simply defined as the applied gate-to-source voltage needed to turn-on a MOS device. For a uniformly doped long channel device, the threshold voltage can be approximated by solving the one-dimensional Poisson's equation below:

- For an n-channel device

$$V_T = V_{FB} + 2|\varphi_p| + \frac{1}{C_i}\sqrt{2\varepsilon_s q N_a(2|\varphi_p| - V_B)}$$

- For a p-channel device

$$V_T = V_{FB} - 2|\varphi_n| - \frac{1}{C_i}\sqrt{2\varepsilon_s q N_d(2|\varphi_n| + V_B)}$$

Where: V_{FB} is the flat-band voltage, C_i is the insulator capacitance, q is charge carrier density, ε_s is the dielectric permittivity of the semiconductor and V_B is the bulk bias.

While $\varphi_n = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right)$ and $\varphi_p = -\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$

Here φ_n and φ_p are Fermi potentials of the n- and p-channel MOS device structures; N_d and N_a are the acceptor and donor dopant concentrations in the substrates respectively, k is Boltzmann constant, T is the absolute temperature and n_i is the intrinsic electron density.

The threshold voltages are result of the second derivative of the drain current function. The derivative at a point is computed by taking the average of the slopes between the point and its two closest neighbors. A summary of the computed threshold and sub-threshold values is shown in Table 1 below.

Table 1. Threshold and sub-threshold values

Mobility Model	Threshold Voltage (V)	Sub-Threshold Voltage (V/decade)
CVT Mobility Model	0.612437	0.0889462
Modified Watt Mobility Model	0.563719	0.088832
Klaassen Mobility Model	0.560913	0.0888324
Yamaguchi Mobility Model	0.602621	0.088692

The fabricated strained-Si model was tested and produced the I-V curves shown in Fig. 4.

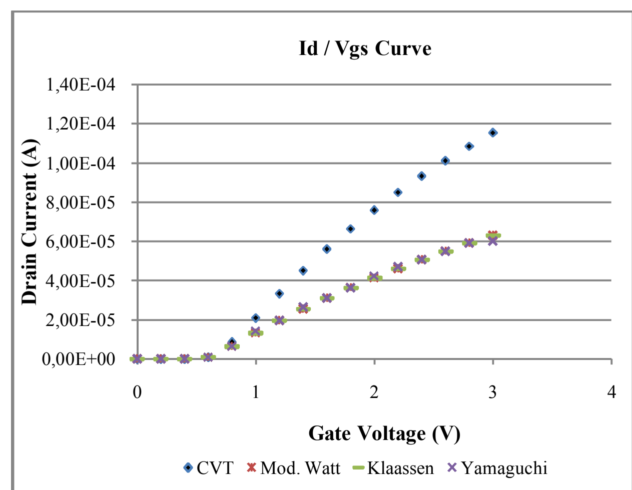

Fig. 4 – Device I-V Characteristics

The figure shows that most models present close drain currents I_d using the default parameters for the described device except for the CVT model that shows higher current levels. This behavior results from the fact that the Lombardi CVT model starts with a higher initial mobility for electron. This behavior can be adjusted by combining it with a model such as the Shirahata mobility model.

6.2. CARRIER CONCENTRATIONS

The charge carriers in semiconductors are electrons and holes. Their numbers are controlled by the concentrations of impurity elements, that is, the doping concentration. Therefore the doping concentration has huge influence on carrier mobility. When modeling the drain current of strained-Si in n-MOSFETs, it is often useful to compute suitable expressions for the carrier concentrations as a function of gate voltage V_{gs} as shown in Fig. 5. It can clearly be observed that, just as in enhancement mode and depletion mode MOSFET, the channel carrier density can be controlled by the gate voltage in exactly the same manner with a proper gated structure. The figure shows that the concentration of carriers in structure layer is proportional to the gate voltage. This behavior is replicated across all mobility models and seems to be more pronounced in the Lombardi CVT model.

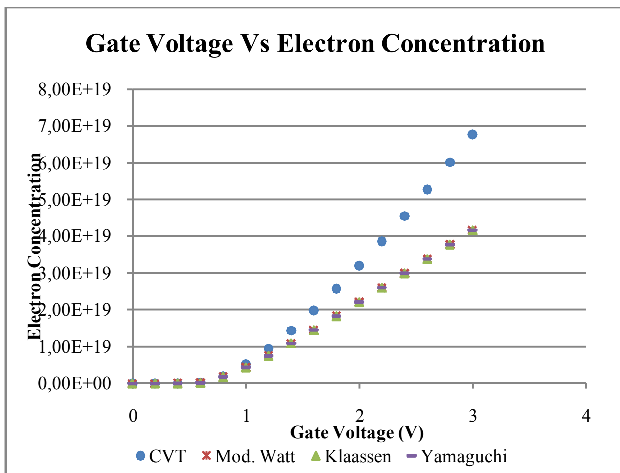

Fig. 5 – Electron Concentration as a function of Gate Voltage

It is worth mentioning at this stage that throughout the experiments and simulations, it was observed that the threshold voltage is strongly dependent on the doping concentration. As we increased the doping level, the threshold voltage became more positive for an n-channel and more negative in a p-channel device. As V_{gs} increases above the threshold voltage V_{TH}, a layer of conduction electrons forms at the substrate surface.

6.3. ELECTRON MOBILITY

Since early 90's, strained-Si on silicon substrates is being carefully explored as a promising alternative to boosting CMOS performance [23 - 25]. The mobility advantage the strain offers at no significant processing cost makes it an ideal candidate for performance enhanced devices. Until now, the substrate-induced biaxial strain has produced the best results for long channel at low electric field and high strain.

To effectively model carrier mobility in the high, low or inversion layers, a description of both roughness scattering and impurity scattering is required. The former dominates the transport at high effective electric field and the latter strongly varies as a function of the effective electric field.

A plot of the Electric field vs Electron mobility for the high, low and inversion layers is shown in Fig. 6. The simulated results are in excellent agreement with the universal mobility curve computed by Takagi et al. [26]. Clearly, mobility decreases with increasing channel field. This behavior is attributed to impurities and defects that cause electron scattering or collisions. Under high electric field, electrons are distributed close to the SiO_2/Si interface, and the probability for an electron undergoing a diffusive scattering event increases for a given period of time.

In Fig. 6, it can be observed that for high channel field values, surface-roughness scatterings are dominant and independent of the doping level, leading to a decrease of the channel mobility. This behavior is observed for all mobility models except for the Yamaguchi model that seem to display a constant behavior under all channel field values.

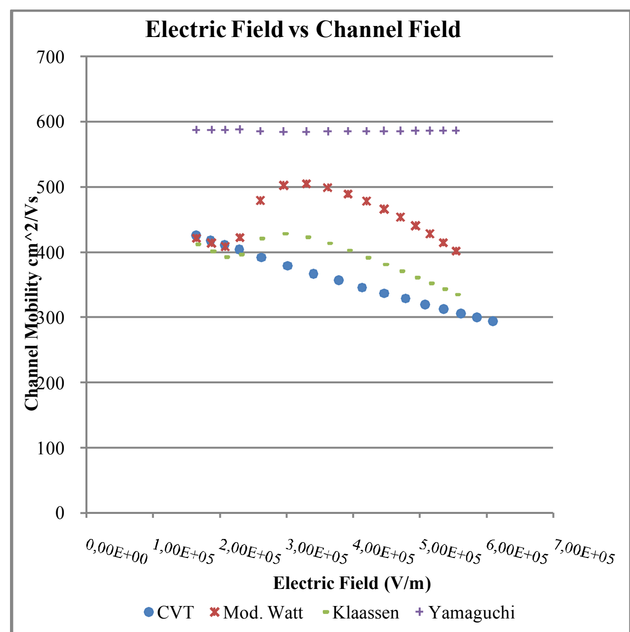

Fig. 6 – Channel Mobility vs Channel Field

At low gate voltage V_G, the channel mobility decreases as the electron concentration increases. This is illustrated in Fig. 7. Such a behavior is a clear indication of the fact that impurities scatterings becomes a lot more frequent when the doping level is high.

Our simulated model was then compared with several empirical and semi-empirical mobility models reported in [27] and it became evident that in the nano-scale regime, the mobility of carriers can be increased by using the strained silicon technology.

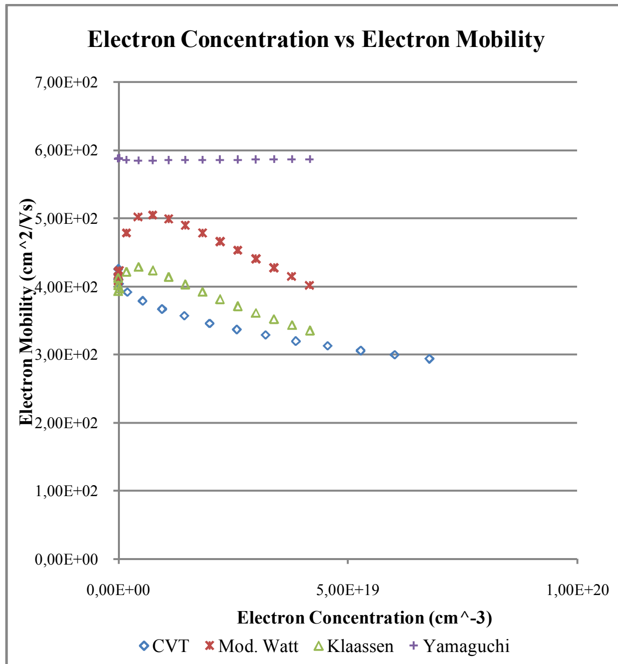

Fig. 7 – Channel Mobility vs Electron Concentration

6.4. HOLE MOBILITY

An analogous study for hole mobility in strained silicon MOSFETs devices was also conducted and the results are shown in Fig. 8. Holes are fictitious and are considered as absence of electrons. From the Fig. 8 it is evident that the hole mobility is less than that of electron. This is due to the fact that the mobility is inversely proportional to the effective mass and the effective mass of hole is much higher than that of electron. Thus the electron mobility is higher than that of hole. Furthermore, electrons travel in the conduction band while holes travel in the valence band. In an applied electric field, holes cannot move as freely as electrons because their movements are restricted. Therefore mobility of a particle in a semiconductor is larger if its effective mass is smaller and the time between scattering events is larger.

Clearly, strain influences each type of charge carrier (holes and electrons) differently in low, high or inversion layers. In both the Yamaguchi and the modified Watt mobility models, hole mobility appears to be constant and independent of the electric field variations.

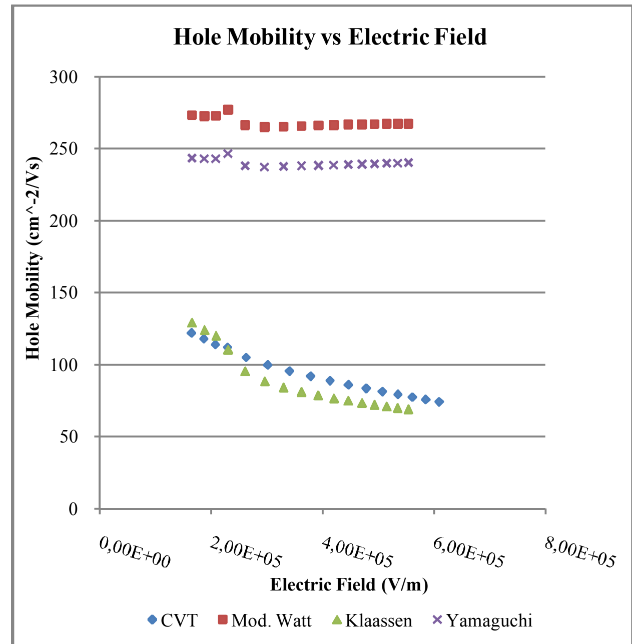

Fig. 8 – Channel Mobility vs Electron Concentration

In the Klaassen and Lombardy CVT models however, an increase in the electric field is translated to a decrease in the hole mobility; this is directly related to collisions with impurities and lattice vibrations. During simulations it was noticed that a selectively deposited SiGe source/drain structure induced compression in the channel in PMOS devices, improving hole mobility. In Si-strain technology, the interatomic distances in the silicon crystal are stretched, generally increasing the mobility of electrons making n-type transistors faster. P-type transistors, in which holes are the majority charge carriers, are not significantly enhanced with tensile stress and, in some cases, their mobility can be reduced. However, the mobility of holes can be increased dramatically by compressive stress where the interatomic distances are shortened.

6.5. DEVICE TRANSCONDUCTANCE

One of the measures of quality for device mobility is transconductance. It is a measure of how the drain current will change with a change in the gate voltage. Mathematically, transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_g} = \frac{\mu C W}{L}(V_g - V_t)$$

Where μ is the carrier mobility, C is the gate capacitance, W is the gate width, and L is the gate length.

Fig. 9 represents the transconductance as a function of the intrinsic drain voltage V_d for a series of intrinsic gate voltage V_g. In the figure, it can be noticed that the transconductance increases rapidly as the gate voltage increases until the saturation regime is reached where the transconductance is saturated. This behavior can be explained by the fact that as the gate voltage increases in absolute value, the greater the width of area of space charge. The extension of this area ends when it occupies all the width within the channel at this stage no passage of current is then theoretically possible. As the gate voltage is further increase, the transconductance drops sharply.

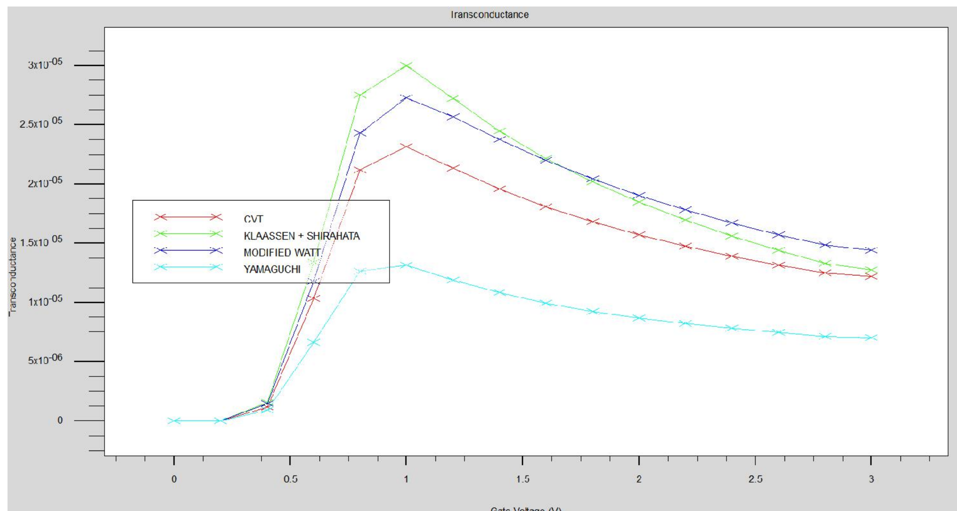

Fig. 9 – Transconductance

This behavior is observed in all mobility layers although less pronounced in the Yamaguchi model.

6.6. ELECTRON VELOCITY

Mobility by definition dependents on the drift velocity. The main factor determining drift velocity (other than effective mass) is scattering time, i.e. how long the carrier is accelerated by the electric field until it collides with something that changes its direction and/or energy. The most important sources of scattering in typical semiconductor materials are ionized impurity scattering and lattice scattering. When an electric field is applied to a semiconductor, the generated electrostatic force causes the carriers to accelerate and reach a constant average velocity, v_{const}, as a result of the many collisions with impurities. Mobility can also be defined as the ratio of the velocity to the applied field. The carriers' velocity saturates at high electric fields attaining the saturation velocity. Further collisions and scatterings occur when carriers flow at the surface of the semiconductor. This results in a much lower mobility. A plot of electron velocity as a function of the applied electric field is shown in Fig. 10.

This velocity is a characteristic of the material and a strong function of doping or impurity levels and temperature. As the electric field is increased, however, the carrier velocity increases sub-linearly and asymptotically towards a maximum possible value, called the saturation velocity V_{sat}.

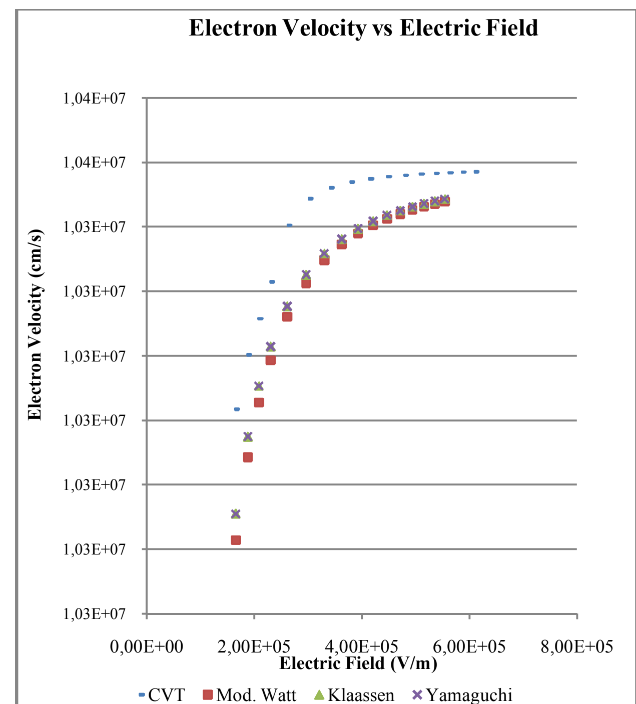

Fig. 10 – Electron velocity in the applied electric field

This velocity saturation phenomenon originates from a process known as optical phonon scattering. At higher electric fields, carriers are accelerated enough to acquire adequate kinetic energy between collisions to transmit an optical phonon; they go through that process very quickly before being accelerated once again.

Beside velocity saturation as a possible high-field behavior, an analogous effect is known as Gunn Effect. In the Gunn Effect, a high enough electric field can produce inter-valley electron transfer. This has the effect of reducing the drift velocity. Increasing the electric field almost always raises the drift velocity, or leaves it unaltered. The outcome is usually negative differential resistance. Clearly, mobility is a strong function of electric field in the regime of velocity saturation. At low fields, the drift velocity is a function of the electric field, thus the mobility is constant.

7. CONCLUSION

In this work, a comprehensive investigation of the effect of carrier mobility, carrier concentrations, transconductance, and electron velocity in strained-Si devices was carried out in order to characterize and optimize CMOS transistor design to produce results that better fit the experimental curves. The validity of the simulated model was established by simulating the Ids, gm and Gd characteristics. The performance of the model was compared with experimental results existing in the literature by calculating the characteristics of the fabricated device. It was demonstrated that the proposed model is a comprehensive one capable of simulating DC characteristics of strained silicon devices. It was shown that charge carriers in semiconductors are electrons and holes and that their numbers are controlled by the concentrations of impurity elements, i.e. doping concentration and for that reason doping concentration has great influence on carrier mobility. We also demonstrated that mobility decreases with increasing channel field. This behavior is attributed to impurities and defects that cause electron scattering or collisions. As for holes, it was shown that holes are fictitious and are considered as absence of electrons. Their mobility is less than that of electron. This is due to the fact that the mobility is inversely proportional to the effective mass. The effective mass of hole on the other hand is much higher than that of electron. Therefore the electron mobility is much higher than that of hole. In both the Yamaguchi and the modified Watt mobility layers, hole mobility appeared to be constant and independent of the electric field variations. In the Klaassen and Lombardy CVT models however, an increase in the electric field was translates to a decrease in the hole mobility. The transconductance was seen to be a function of the intrinsic gate voltage

8. REFERENCES

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