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ANALYSIS AND PERSPECTIVES FOR THE DEVELOPMENT OF DIGITAL SYNTHESIZERS OF DIRECT SYNTHESIS OF FREQUENCY

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The stages of modern digital frequency synthesizers of direct synthesis development have been analyzed. The structural diagram of a classical digital synthesizer and its mathematical model have been reviewed, which allowed to analyze the distortions causes in synthesized signals. The ways of further development using the latest high-frequency semiconductor technologies have been researched.

Keywords*: DFS, phase accumulator, stages of development, semiconductor technologies.*

Problem statement and publications analysis. Digital frequency synthesizers (DFS) of direct synthesis are widely used in various radio equipment. This situation makes it urgent to develop new and more advanced synthesizers and to improve already known signal synthesis systems. Frequency synthesizers should carry out operative, as fast as possible frequency adjustments in accordance with the control codes received from external sources of control, while providing the necessary parameters in the range of operating frequencies, type of modulation, resolution, phase noise level and the side components in the output signal spectrum.

Digital frequency synthesizers are used both in formation signals devices and in receiving and processing signals devices [1 - 4].

Synthesizers are widely used in various satellite communication systems, radar and radionavigation systems, measuring generators, and so on, whereby phase and frequency modulation, which are realized directly in the structure of the DFS, as well as high reliability.

Several stages of the DFS development. The first stage let's call the period from the early 70's to the early 80's of the twentieth century. Computing synthesizers were mostly objects of theoretical researches during this period of time, and practically realized samples had clock frequencies about one megahertz. This circumstance was dictated by the level of the digital and analog elemental base development.

The second stage, from the early 80's to the early 90's of the 20th century, was marked by the rapid development of digital technologies in various fields of technology. During this period of time, integrated technologies were developed: CMOS, SOS, GaAs, ECL. The production of chips based on these technologies allowed them to work with a clock frequency of tens of megahertz. The main manufacturers were Qualcomm, Harris, Huges Space and Communication Company, Texas Instruments, Analog Devices, Motorola, Plessey, Stanford Telecom, Rockwell.

The third stage - from the early 90's of the twentieth century to the beginning of the 2000s, characterized by the period of the main structural DFS schemes formation, the creation of new algorithms for the operation of functional blocks, as well as developing digital-analog devices with a clock speed of hundreds and thousands of megahertz.

During this period of time, Analog Devices, which is currently the leader in this industry, has come out on leading positions in the production of DFS based on the CMOS technology. The products of this company have quite high quality, variety and relatively high availability. This can not be said about other manufacturers.

The fourth stage in the DFS development - from the beginning of the twenty-first century till the present times - characterizes significant efforts and a large volume of work on the creation of high-frequency DFS.

The next stage of the DFS development will start after the beginning of the high-frequency DFS with output frequencies up to 20 GHz industrial release.

The purpose of the article is to analyze the trends of perspective high-frequency DFS development based on the latest semiconductor technologies.

The main material. The structure of the digital frequency synthesizer has not changed significantly since the first publications. In general, the DFS (with the exception of various correction schemes) contains: a clock reference, a phase accumulator, a phase to sinusoid amplitude converter (DSP), a digital-to-analog converter (DAC) and bandpass filter (LPF) (Fig. 1).

The main node of the DFS is a phase accumulator (containing adder and register). It works as an address generator for addressing of a read-only memory device (ROM), which contains samples of a synthesized function, usually trigonometric.

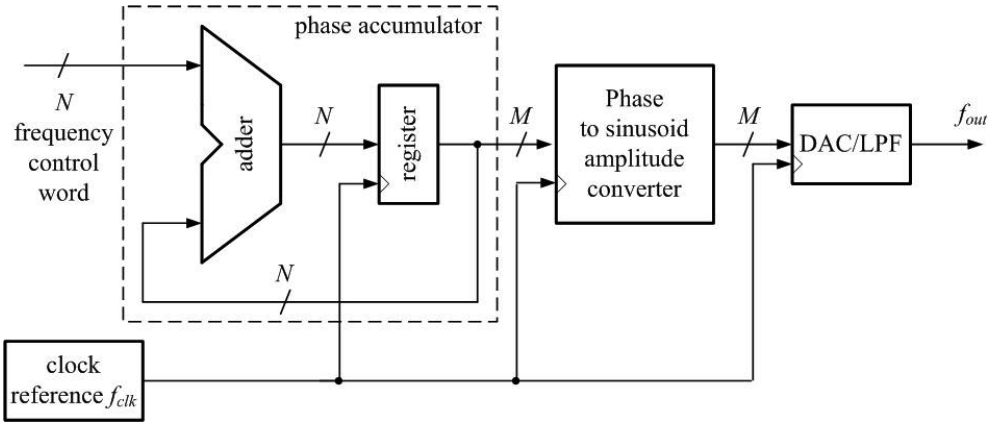

Fig. 1. Structural diagram of the classical DFS

The process of frequency synthesis is as follows. A phase accumulator generates a phase code which value changes linearly with a step equal to the frequency code N and is converted into an amplitude code according to the table function of the sinus contained in the ROM. Then, based on the amplitude code, the DAC forms an analog

signal that, after filtering in the LPF, takes the required harmonic form. Thus, the frequency of the output synthesized signal is determined by the expression:

$$f_{out} = \frac{N}{2^m} \cdot f_{clk},$$

where m –the phase accumulator capacity,
f_{clk} – the clock frequency.

The synthesized frequency step change

$$\Delta f = \frac{f_{clk}}{2^m}.$$

For example, if the clock frequency is 25 MHz and the phase accumulator capacity is m = 28, then the frequency step change will be 0.0931 Hz. It's possible to reduce the adjusting frequency step by increasing the phase accumulator capacity.

Serially produced DFSs phase accumulators have a capacity of 28, 32, or 48 bits, but only part of them M (senior grades) is used to address the ROM. This is done due to the need to reduce the size of the ROM. If you use, for example, 32 bits of the ROM address and ten-bit representation of each count, then it's necessary to have a ROM of 232 × 10 = 42949672960 ≈ 43 GBs.

To reduce the capacity of the ROM, one can use the special features of the sin function symmetry. In the DFSs' majority in the ROM there is only one quarter of the period, but thus the logic of the ROM address formation is complicated.

Taking into account certain features of the synthesizer different nodes functioning in the spectrum of the output signal, there are unwanted discrete components, which have sometimes quite significant amplitude.

In Figure 2. a functional diagram of the mathematical model of the DFS is presented, where e_1 is an error caused by the rounding of the phase when addressing the ROM; e_2 is an error associated with the finite bit of the data bus; e_3 is an error caused by a non-linearity of a digital-to-analog converter (DAC), its own noise and switching interference DAC; $W_1(x)$ - error e_1 compensation device; $W_2(x)$ - error e_2 compensation device.

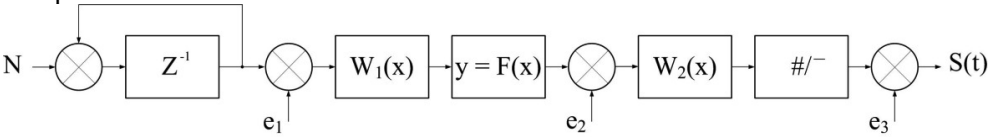

Fig. 2. Functional scheme of DFS mathematical model

The rounding phase error (e_1) occurs while addressing the ROM, which contains the table of the synthesized function, makes the most significant contribution to the deterioration of the synthesizer spectral characteristics, causing the appearance of unwanted discrete components in the output signal spectrum. Rejecting the junior bits of the address code leads to an error in the representation of the phase, and as a consequence, when the phase is converted to the amplitude of the output signal, an

error occurs. This error is periodic because, depending on the frequency code, the same phase state of the phase accumulator repeats itself often or less frequently. As a result, in the spectrum of the DFS output signal there are discrete components, which are caused by the cutoff of the phase code.

The rounding data error (e_2) can be significantly reduced by increasing the bit number of the data bus ROM, which causes only a linear increase in its capacity.

DAC error (e_3) can be reduced by the choice of sufficiently high-quality DACs, as well as through the use of special circuit design solutions.

The structure of the above discussed DFS scheme (Fig. 1), in addition to the DAC, may also include additional digital blocks:

- multiplier of reference frequency;
- an additional digital adder for programming the phase;
- inverse sinc-filter to compensate the FTC uneven;
- an additional digital multiplier for forming an amplitude-modulated signal;
- an additional DAC for quadrature signals I and Q receiving;
- an additional comparator with a small trembling front ("jitter") for forming a digital clock signal;
- an additional frequency and phase registers that can be programmed for frequency or phase manipulation.

From the past twenty years and to the present time, in the USA, in particular, there are active researches and development in the field of high-frequency DFSs. For instance, in the United States the task for DFS with output frequencies up to 20 GHz creating in the future is set.

High-frequency DFSs should play a significant role in perspective radio engineering systems. Such studies are conducted, first of all, under the auspices of defense departments and organizations in the United States.

Not so long time ago, a number of papers were published, in which laboratory samples of high-frequency DFSs microchips with a clock speed of up to 32 GHz, performed on the basis of perspective semiconductor technologies, were presented.

The appearance of high-frequency DFS in the market will lead to the rapid development and introduction of a radio equipment and systems new generation, primarily new radars and digital active phase antenna arrays (CAFAR).

A number of companies, obviously, in the long run will create different devices based on serial high-frequency DFSs. At the same time, at this stage, probably, work on the creation of DFS microchips with output frequencies from 20 to 30 GHz and above will be carried out.

The clock and output frequencies of these DFSs should be at times and tens times higher than existing commercial ones. For today, in the latest model of the DFS of Analog Devices AD9914, the output synthesized frequency reaches 1.4 GHz at a clock speed of 3.5 GHz.

Consequently, while creating a DFS new generation, developers solve the following tasks:

- increasing of output working frequencies (in the future up to 20 GHz);

- formation of complex signals with necessary parameters;
- extending the frequency range and ensuring the functioning of the DFS in a very wide band of frequencies;
- operative change of parameters;
- improvement of synthesizers spectral characteristics;
- application to synthesizers already tested methods of control and improving the quality of their functionality;
- verification and application of perspective semiconductor technologies as a base for the production of high-speed DFSs and their further development.

It is anticipated that high-speed DFSs will play a decisive role in the construction of radio engineering systems, which will be used in wars with the use of high-precision weapons. For example, such systems include radars of new generation, capable of real-time monitoring various parameters of "complex" purposes, including small size.

Such DFSs, as mentioned above, will play important role in perspective CAFARs creating, which provide digital rays formation and can function in multi- rays mode. In addition, the developed DFS will allow the formation of precise time delays, which will enable the control of the radar rays (technology True Time Delay).

Virtually all US works on perspective DFS are conducted with the support and participation of organizations involved in defense research and development. These include, in particular, the Defense Advanced Research Projects Agency (DARPA) and U.S. Army Research Laboratory. Many developments in promising DFS are carried out under the general program for military agencies (Technology for Frequency Agile Digitally Synthesized Transmitters - TFAST technology for transmitting devices with fast digital syntheses of frequencies and signals) [5 - 8].

It is proposed to use high-frequency semiconductor technologies for the development and manufacturing of advanced DFS.

First of all, they include technology based on InP (Phosphide India) and SiGe (Silicon Germanium). Both of these technologies allow you to get the transistor limit frequencies and the maximum frequency of power amplification much higher than 100 GHz.

For example, for InP technology, the limiting frequency and gain may reach 300 GHz. For the SiGe technology, the limiting and amplified frequencies can exceed the value of 200 GHz.

As follows from the given sources [5-8], the fastest laboratory samples of perspective DFS are made using InP technology. However, the number of InP chips which are used for work, is less than that of SiGe-based technology. Using the SiGe technology, you can get more compact elements, with less power and, consequently, less cost.

From the publications analysis in recent years, it follows that both of these technologies are developing and competing and will be the basis for the release of prospective DFSs. For example, the modifications of technology based on InP can significantly reduce the power consumption and reduce the width of the emitter to a value of 0.15 microns, which increases the number of transistors per chip by one order (to about 20,000 and more).

Recently, more high-frequency microchipes of the DFSs have also been used on the basis of SiGe technology.

But the technology based on GaAs (Arsenide Gaul) on a frequency of several times loses to InP and SiGe technology, so over the past few years, has practically not been used in the development of high-frequency DFSs.

Conclusions. The analysis of a significant number of perspective DFSs developments has showed that by the beginning of the second decade of the twenty first century, in this issue has been achieved considerable success.

Thus the clock speed of the DFS reached a value of 32 GHz, and the output frequency was 16 GHz (prototype samples).

Three main technologies are used by the high-frequency DFS manufacturers nowadays - based on InP, SiGe and GaAs.

Two main approaches to their structure are developed and competing at the same time in the high-speed DFSs designing and developing – with and without using the ROM. In DFS without ROM, in most cases, a nonlinear DAC is used, which solves the problem of a harmonic signal forming and a digital-to-analog conversion.

At present, considerable attention in the perspective DFSs development is given not to the expansion of the frequency range, but to a deeper elaboration of the DFS scheme in general. The main task here is to provide quality indicators for digital frequency synthesizers. Most likely, various methods of increasing effectiveness, which are already being used in structures of existing DFSs, will be actively used. For example, randomization of parasitic components in DFSs.

In conclusion, we can assume that it will take a long time to refine existing samples of new digital signal synthesizers, to improve their structures, to verify experimentally and to create on their basis high-speed high-frequency synthesizers of frequencies and signals, which will subsequently be produced serially.

REFERENCES

1. Tierney J., Rader C.M., Gold B. (1971), A Digital Frequency Synthesizer / Tierney J., Rader C.M., Gold B. // IEEE Trans. Audio Electroacoust, vol. Au-19 № 1, pp. 48 - 57, (in English).
2. Kroupa V. F. (1998), Direct Digital Frequency Synthesizers / V. F. Kroupa // New York, IEEE Reprint Press Book. – 1998. – 364 pp. (in English).
3. Jouko Vankka (2001), Direct Digital Synthesizers: Theory, Design and Applications / Jouko Vankka // Boston; London: Kluwer Academic Publishers. – 2001. – pp. 216. (in English).
4. Stakhiv R.I. (2003), Tsyfrovi syntezatory chastoty / Stakhiv R.I. // Komp'iuterni tekhnolohii drukarstva: zb. nauk. prats. – Lviv: UAD. - № 10. S. 138-145. (in Ukrainian).
5. Steven Eugene Turne, Richard T. Chan, and Jeffrey T. Feng (2008), ROM-Base Direct Digital Synthesizer at 24 GHz Clock Frequency in InP DHBT Technology / Steven Eugene Turner, Member, IEEE, Richard T. Chan, and Jeffrey T. Feng, Member, IEEE. // IEEE Microwave and Wireless Components Letters, August 2008, Vol. 18, №. 8, pp. 566 – 568, (in English).

6. Xuefeng Yu, Fa Foster Dai, Senior Member, J. David Irwin, Life Fellow and Richard C. Jaeger, Fellow (2008), A 12 GHz 1.9 W Direct Digital Synthesizer MMIC Implemented in 0.18μm SiGe BiCMOS Technology / Xuefeng Yu, Fa Foster Dai, Senior Member, IEEE, J. David Irwin, Life Fellow, IEEE, and Richard C. Jaeger, Fellow, IEEE // IEEE Jornal of Solid – State Circuits, June 2008, VOL. 43, № 6, pp. 1384 – 1393, (in English).
7. Steven Eugene Turner, Student Member, and David E. Kotecki, (2006), Direct Digital Synthesizer With Sine – Weighted DAC at 32 – GHz Clock Frequency in InP DHBT Technology / Steven Eugene Turner, Student Member, IEEE, and David E. Kotecki, Senior Member IEEE // IEEE Journal of Solid – State Circuits, October 2006, VOL. 41, № 10, pp 2284-2290, (in English).
8. Xueyang Geng, Fa Foster Dai, Fellow, J. David Irwin, and Richard C. Jaeger, (2010), 24 – Bit 5.0 GHz Direct Digital Synthesizer RFIC With Direct Digital Modulations in 0.13 μm SiGe BiCMOS Technology // Xueyang Geng, Student Member, IEEE, Fa Foster Dai, Fellow, IEEE, J. David Irwin, Life Fellow, IEEE, and Richard C. Jaeger, Life Fellow, IEEE // IEEE Journal of Solid – State Circuits, May 2010, VOL. 45, № 5, pp 944-954, (in English).

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АНАЛІЗ ТА ПЕРСПЕКТИВИ РОЗВИТКУ ЦИФРОВИХ СИНТЕЗАТОРІВ ПРЯМОГО СИНТЕЗУ ЧАСТОТИ

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Проаналізовані етапи розвитку сучасних цифрових синтезаторів прямого синтезу частоти. Розглянуто структурну схему класичного цифрового синтезатора та її математичну модель, що дозволило проаналізувати причини спотворень у синтезованих сигналах. Досліджені шляхи подальшого розвитку з використанням новітніх високочастотних напівпровідникових технологій.

***Ключові слова**: ЦСЧ, фазовий акумулятор, етапи розвитку, напівпровідникові технології.*

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