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Determination of interface state density in high-*k* dielectric-silicon system from conductance-frequency measurements

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Abstract. Capacitance-voltage (*C*-*V*) and conductance-frequency (*G*-ω) techniques were modified in order to take into account the leakage current flowing through the metal-oxide-semiconductor (MOS) structure. The results of measurements of interface state densities in several high$-k$ dielectric – silicon systems, including transition metal (Hf) and rare-earth metal (Gd, Nd) oxides, ternary compounds ($LaLuO_3$) and silicate ($LaSiO_x$), are presented. It was shown that the interface state densities can be as low as $(1.5...2)\times 10^{11}\,\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ for Al-HfO_2-Si, Pt-Gd_2O_3-Si and Pt-$LaLuO_3$-Si systems if the dielectric layer is deposited onto (100) silicon wafer surface. The electrically active states are attributed presumably to silicon dangling bonds at the interface between dielectric and semiconductor.

Keywords: high-*k* dielectric, dielectric-semiconductor interface.

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1. Introduction

Dielectrics with a high dielectric constant (high$-k$ dielectrics) are currently considered as a replacement of silicon dioxide in complementary metal-oxide-semiconductor (CMOS) technology. The continuing downscaling of MOS devices requires respective thinning of gate dielectrics. However, the reduction of SiO_2 thickness below 1.5 nm is associated with several critical drawbacks, the most important of which is an increased leakage current through the gate oxide. In order to reduce gate leakage while maintaining the gate capacitance, dielectrics with higher permittivity than SiO_2, the so-called high$-k$ dielectrics, are being intensively investigated now. High$-k$ dielectrics can be grown thicker than silicon oxide providing the same capacitance equivalent thickness (CET) and offering significant gate leakage reduction due to suppressing the direct tunneling effects.

Transition metal and rare-earth metal oxides are considered as perspective high$-k$ materials to replace silicon dioxide for future CMOS technology because of their wide bandgap and large offsets between conductance and valence bands of dielectric and silicon. Among the high$-k$ dielectrics, HfO_2 is the most promising candidate because of its relatively high dielectric constant, large bandgap, and thermal stability. The comprehensive reviews of future high$-k$ dielectrics for substitution of silicon dioxide can be found in [1 – 4]. The electrical properties of the high$-k$ oxide/silicon structures, such as leakage current and band offsets, were found to depend also on the chemical composition of the transition layer at the interface [5]. The use of epitaxially grown single-crystalline thin layers of rare-earth oxide dielectric allows us to solve two problems: first, to reduce thickness of the transition layer between silicon and high$-k$ dielectric [6] and, second, to decrease the leakage current through grain boundaries that are generated during crystallization of the amorphous dielectric layer at high-temperature technological processes [7].

The investigations of interface states are of interest, first of all, because low densities of the interface states are required to provide an appropriate channel mobility of CMOS devices and to guarantee the precise control of the surface potential under the gate. However, even with the perfect crystalline quality of the dielectric layer and abrupt oxide/silicon interface, the achievement of low

Table. Parameters of the samples.

Sample #	Oxide layer	Substrate	Forming gas annealing	Thickness, nm	CET, nm	k
1	Gd_2O_3	pSi (111)	500 °C/10 min	6.7	2.35	11.2
2	Gd_2O_3	pSi (100)	450 °C/10 min	7.5	2.5	11.7
3	Gd_2O_3	pSi (111)	450 °C/10 min	13.2	4.5	11.5
4	Nd_2O_3	pSi (111)	450 °C/10 min	10.0	3.2	11.9

leakage currents in high $-k$ dielectric – silicon systems is a problem, because the rare-earth oxides, like to most of types of high $-k$ dielectrics, are ionic compounds with relatively weak chemical bonds between ions, and are known to contain a high concentration of oxygen vacancies [1]. These intrinsic defects produce the local energy levels in the bandgap, being a reason of relatively high leakage currents. In this case, the charge carrier exchange between the dielectric and semiconductor essentially depends on the presence and density of surface states at the interface. This is the second reason why the studies of properties inherent to the interface states in the high $-k$ dielectric – semiconductor system are of interest.

Application of conductance-frequency spectroscopy to characterization of high $-k$ -oxide/silicon interface and possible nature of interface defects of several high $-k$ systems were discussed in [4, 8–10]. However, this technique was not commonly used for the study of interface properties in the case when a high leakage current flows through the dielectric film. In this paper, the measurement technique was modified to account for possible leakage currents. This paper presents the results of capacitance-voltage and ac conductance-frequency measurements for several high $-k$ dielectrics, including transition metal (Hf) and rare-earth metal (Gd, Nd) oxides, ternary compounds ($LaLuO_3$) and silicate ($LaSiO_x$), epitaxially grown on silicon substrates.

2. Experimental

The HfO_2 films were deposited on fresh un-etched p-type Si(100) substrate with the resistivity of $1...10\,\mathrm{Ohm}\cdot\mathrm{cm}$. Films were deposited at 500 °C by liquid injection MOCVD, using the Aixtron AIX 200FE Atomic Vapour Deposition (AVD) reactor fitted with the "Trijet"™ injector system. The hafnium precursor was $Hf(mmp)_4$. The wafers were HF cleaned before the deposition. The metal gate electrodes were deposited by sputtering to fabricate MIS capacitors. The nitride gates were reactively sputtered in Ar/N flow, the silicidation process of the NiSi gate was performed in argon at 500 °C for 10 s. The thickness of metal and metal compound layers was 50 nm. The standard lift-off process was used to pattern the conducting films to define the circular dots. Then the samples were annealed in forming gas at 400 °C for 30 min. The samples with four different gate materials, NiAlN, TiN, NiSi, and Al, were investigated.

The single-crystalline Gd and Nd oxide films were grown in an integrated multichamber ultrahigh vacuum system using solid source molecular beam epitaxy (MBE), which allows better control of semiconductor/dielectric interface properties and to avoid a low dielectric constant interfacial layer. The details of deposition of metal oxide dielectric films can be found elsewhere [14]. Prior to Pt metal dot deposition, the structures were annealed in forming gas for 10 min at 450 or 500 °C to decrease the charge instability in dielectrics [14]. Four different structures were studied: Pt-Gd_2O_3-pSi(111) annealed at 500 °C (hereafter denoted as #1), Pt-Gd_2O_3-pSi(100) annealed at 450 °C (#2), Pt-Gd_2O_3-pSi(111) annealed at 450 °C (#3), and Pt-Nd_2O_3-pSi(111) annealed at 450 °C (#4). The chemical composition of dielectric layers, details of their preparation and some parameters are shown in Table.

The dielectric layers in the Pt-$LaLuO_3$-pSi(100) MOS structures were deposited by molecular beam deposition (MBD). Evaporation of La and Lu in O_2 was performed at a substrate temperature of 450 °C. Two structures were studied with the nominal physical thicknesses of the dielectric layer ($LaLuO_3$) of t_{ox} = 6.5 nm and 20 nm. The samples were exposed to forming gas annealing at 400 °C for 10 min (10% H_2). Pt gates were prepared by e-gun evaporation through a shadow mask.

The dielectric layers of the NiSi-$LaSiO_x$-Si(100) MOS structures were deposited onto *n*- and *p*-type silicon substrates by electron beam evaporation from La_2O_3 pellets [5]. The structures were studied with the nominal physical thicknesses of the dielectric layer ($LaSiO_x$) of t_{ox} = 10 nm and 7.5 nm. Circular NiSi electrodes have been fabricated by full silicidation and reactive ion etching [6]. The samples obtained no post-metallization annealing treatment.

MOS capacitors were characterized by capacitance-voltage (C-V), conductance vs. frequency (G-ω) measurements within the temperature range 120 up to 320 K using an Agilent 4284A LCR meter.

3. Measurement techniques

One of general problems in *C-V* characterization of ultra-thin SiO_2 and alternative dielectric layers is a large leakage current, leading to the appearance of parasitic resistance of back contact and semiconductor bulk. These effects lead to underestimation of the true capacitance in accumulation region, if the *C-V* curve is measured in the parallel mode [11, 12]. The correct *C-V* dependence can be extracted from *C-V* data measured at two different frequencies using the approach described in [13]. In this case, the resistance is given by:

$$R_p = \frac{1}{\sqrt{\omega^2 C'C(1+D'^2) - \omega^2 C^2}}, \qquad (1)$$

where $D' = \frac{1}{\omega R' C'}$, R' and C' are measured resistance and capacitance, respectively, and the corrected capacitance equals:

$$C = \frac{f_1^2 C_1'(1+D_1'^2) - f_2^2 C_2'(1+D_2'^2)}{f_1^2 - f_2^2}. \qquad (2)$$

Here, subscripts 1 and 2 denote two different measuring frequencies. For the case of measurements at two frequencies in the series mode respective equations can be modified as follows:

$$C = \frac{f_1^2 C_{s1}' - f_2^2 C_{s2}'}{f_1^2 - f_2^2}. \qquad (3)$$

The interface state density was determined from the conductance-frequency measurements using the classical approach of Nicollian and Goetzberger [14, 15]. This technique proved its effectiveness and precision and has become a standard for studying the electrically active states at the dielectric/semiconductor interface for at least last four decades. However, it was primarily developed for the SiO_2/Si systems with a relatively thick dielectric layer and relatively low leakage currents. The comprehensive analysis of advantages and restrictions of the *G*-ω technique, in particular in its application to measurements of interface states in the structures with high $-k$ dielectrics, can be found in [9, 10].

Fig. 1 presents the equivalent circuits suggested for modeling the processes and for extracting the density of states from the measured admittance of the total MOS system. Fig. 1a shows the circuit consisting of the measured capacitance C_m and conductance G_m, connected in parallel, just as it is assumed by the LCR-meter to be placed between its testing leads. Nicollian and Goetzberger suggested that MOS structure can be represented by the circuit with the oxide capacitance C_{ox}, the capacitance of the depletion layer of semiconductor C_s, and the capacitance C_{it} and conductance G_{it} of the interface states connected as shown in Fig. 1b [14]. In this case, from the measured dependence of the sample conductance *G* on circular frequency ω of the small ac testing voltage, the concentration of interface states can be determined directly from the peak value of G/ω vs. ω dependence. Fig. 1c shows the equivalent circuit suggested in [9, 10] where some principal remarks were made concerning the interpretation of the results in the case when the density of states or capture cross section has strong energy dependence. However, none of these equivalent circuits takes into consideration the fact that the dielectric layer itself may have significant leakage current, which becomes more important if the thickness of the oxide is small. Therefore, we suggest that an additional oxide conductance G_{ox} should be included into the equivalent circuit as shown in Fig. 1d. Even without writing the cumbersome equations describing the total impedance of this circuit, it is clear that the upper *RC*-circuit at some parameters may give similar contribution to the total measured capacitance and conductance, as the lower one. This may lead to ambiguity in determination of parameters of the interface states, or even to mistaken assignment of the oxide bulk effects to the interface-related processes.

In the case of dielectric layers with leakage currents, the results of both *C-V* and *G*-ω

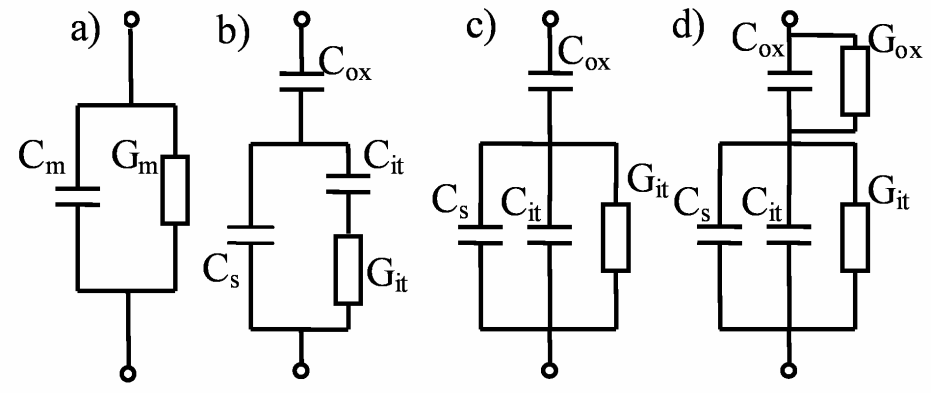

Fig. 1. Equivalent circuits: a) with circuit elements as measured, b) suggested by Nicollian and Goetzberger, c) suggested by J. Piscator et al., and d) with the oxide conductivity included.

measurements require correction, as described in [16]. Before the conductance related to interface traps is plotted in G/ω vs. frequency coordinates, the dc conductance (or the conductance at the minimum frequency) should be subtracted from the measured value in order to get rid of the current component due to leakage through the dielectric layer. The similar approach is used also for studying the distribution of defects in semiconductor heterojunctions by using the admittance technique [17].

4. Results and discussion

Polysilicon has been the gate electrode of the transistor technology for several decades, however, the gate depletion problem becomes a major drawback for its further application. In addition, reaction between the polysilicon gate and high $-k$ dielectric can produce silicides, which affects the dielectric integrity of the gate stack. These reasons justify the investigation of metal and metallic compounds as gate electrodes for CMOS devices.

The distribution of interface traps for the samples with HfO_2 dielectric and three different gate materials (NiAlN, TiN, NiSi) is shown in Fig. 2. The spectrum of interface states is similar for these samples increasing from $3\times10^{11}\,\mathrm{eV^{-1}cm^{-2}}$ in the depth of the bandgap up to $(3.5...5.5)\times10^{12}\,\mathrm{eV^{-1}cm^{-2}}$ closer to the valence band edge. The difference of the gate materials affects mainly the part of the distribution near the bandgap edge. The lowest D_{it} values were observed for NiAlN gate, and the highest – for the TiN gate. Completely different behavior of the distribution of interface states was found for Al-HfO_2-Si structure, as shown in Fig. 3. In this case, the peak of the D_{it} distribution is observed with a maximum at E_V+0.19 eV and with much lower value of the interface trap density, than for other samples at the same energy position. Such a distribution can be attributed to the presence of a local state within the bandgap. The temperature dependence of the capture cross-section for the respective trap is plotted in the inset to Fig. 3.

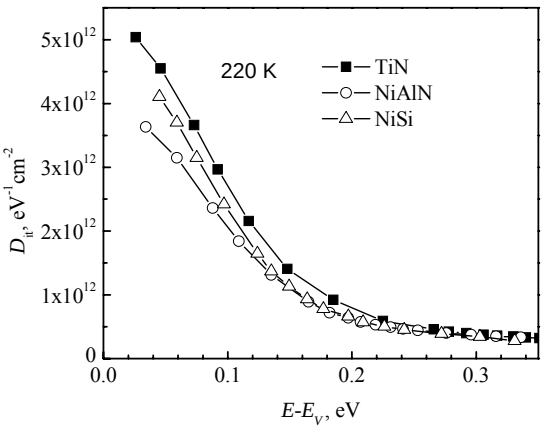

Fig. 2. Interface state spectra for three samples with HfO_2 dielectric and different gate electrodes measured at 220 K.

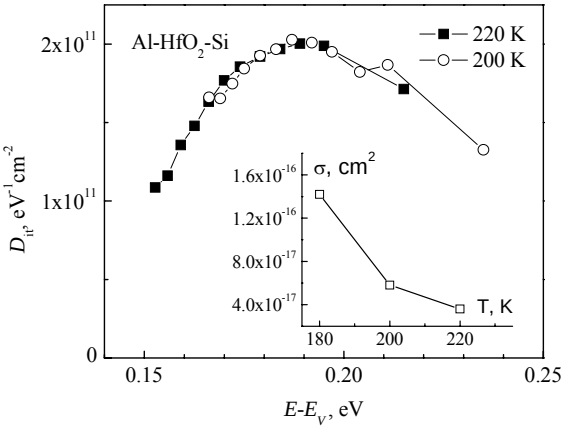

Fig. 3. Interface state spectra for Al-HfO_2-Si structure measured at 200 and 220 K. The inset shows the temperature dependence of the trap capture cross-section.

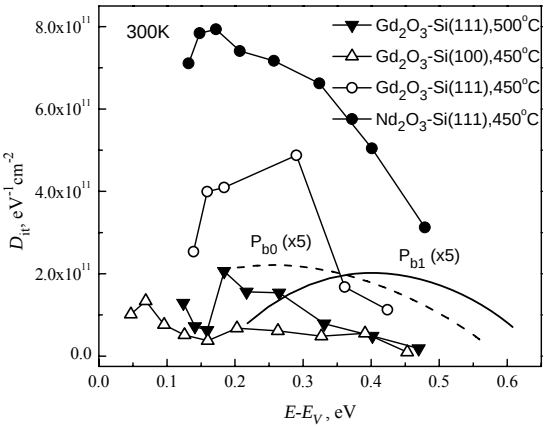

Fig. 4. Interface state density for four samples calculated from G - ω measurements and bandgap distribution of Pb centers on oxidized (100) Si wafer.

Fig. 4 shows the interface state density distribution over the lower part of the bandgap for four samples with Gd and Nd oxide dielectric layers, determined by the standard conductance-frequency (G-ω) technique with subtraction of leakage currents at low frequency. It can be seen that the lowest values are observed on the Gd_2O_3 layer on Si(100) substrate (sample #2), where the average concentration of interface states in the studied energy interval equals to $5\times10^{10}\,\mathrm{eV^{-1}cm^{-2}}$. The highest values are observed in the Nd_2O_3 film, possibly due to a larger lattice mismatch at the interface between the dielectric and semiconductor. Annealing at 500 °C reduces the interface state density by a factor of 2, as compared to that at 450 °C for Gd_2O_3 oxide grown on Si(111) substrate. It should be noted that the maximum concentration of the interface states is observed around $E_t = E_V$+0.20 eV and, in dependence on orientation of Si wafer, around E_V+0.40 eV for Si (100) and E_V+0.30 eV for Si (111). The surface traps with such energy distribution were observed in the SiO_2/Si interface

[18, 19], and the maximum concentration at E_V+0.40 eV was associated with a mixture of P_{b0} and P_{b1} centers and that at E_V+0.30 eV – with P_{b0} centers [20]. Energy distributions of these centers taken from [20] are also depicted in Fig. 4. The concentration of interface states in the (100) silicon surface is much lower than that for (111) surface, the same as it is observed in Si-SiO_2 system, which can be considered as another evidence of formation of intermediate transition region SiO_x between silicon and high $-k$ dielectric. Such an interfacial region can be formed under the high $-k$ oxide due to diffusion of oxygen through the oxide during the deposition process [1]. The lower values of the interface state density for the film grown on Si(100), the significant reduction of D_{it} by higher-temperature forming gas annealing and the higher values of D_{it} for the oxide with larger lattice mismatch enabled us to suggest silicon dangling bond centers as the dominant interface states for the high $-k$ /silicon structures under study. However, the presence of shallower traps may be attributed to the effect of the rare-earth ions on the structure of the transition layer.

Fig. 5 shows the interface density distribution over the lower part of the bandgap for Pt-$LaLuO_3$-Si structures with 6.5 and 20 nm thick dielectric layers. The interface state density is lower for the sample with the thicker oxide, reflecting a better quality of the interface, probably due to presence of a thicker interfacial silicate layer. Typical maxima in the interface state distributions for MOS structures (1.2×10^{11} and $2.5\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$) were found at about 0.25–0.3 eV from the silicon valence band edge.

Fig. 6 shows the distribution of interface state density over silicon bandgap for both *n*- and *p*-type samples with 10 nm $LaSiO_x$ dielectric layer. The middle region corresponds to the values extracted from the conductance technique, while the D_{it} distribution near the edges of bandgap was obtained using the Gray-Brown technique [21]. It should be noted that the two separate approaches yield values of D_{it} which are in good agreement in the energy ranges where these two methods overlap.

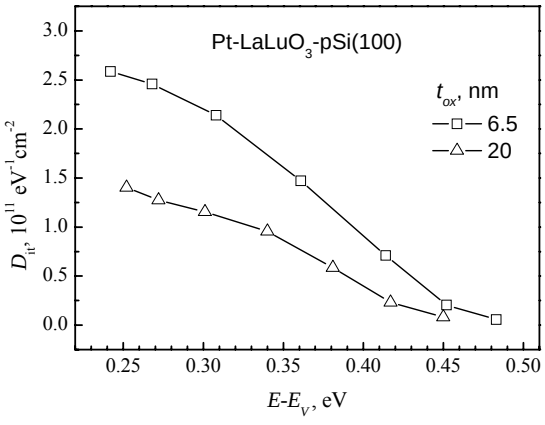

Fig. 5. Interface state density for $LaLuO_3$-Si structures.

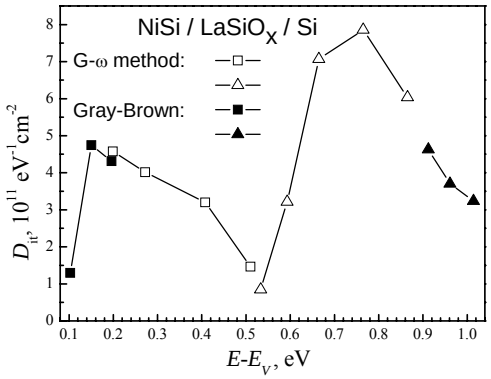

Fig. 6. Interface state density distribution over the silicon bandgap determined using the conductance and Gray-Brown methods.

The maximum values of interface state density were found to be about $4.6\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$ at 0.2 eV above the Si valence band edge and $7.9\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$ at 0.34 eV below the Si conduction band edge. These high values could be expected because no post-metallization annealing was performed. The effective trap cross-sections were found to be equal to 1.3×10^{-16} and $2.3\times10^{-16}\text{cm}^2$ for traps related to the maxima of D_{it} distribution near the valence and conduction bands, respectively. The energy distribution is slightly different from that for P_{b0}/P_{b1} defects, which shows up two maxima at E_V+0.25 eV and E_V+0.83 eV, respectively [4].

It is evident from the presented data that not all of high $-k$ dielectrics under study can approach silicon dioxide in terms of interface states density values. The interface state densities of around $(1.5...2)\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$ were observed in Al-HfO_2-Si, Pt-Gd_2O_3-Si and Pt-$LaLuO_3$-Si systems in the case when the dielectric layer is deposited onto (100) silicon wafer surface. Although these values are still an order of magnitude higher than the best values achieved in SiO_2-Si structures, the operability of MOS transistors with high $-k$ dielectrics was recently demonstrated even for a novel ternary $LaLuO_3$ oxide [22]. The interface state density for $LaSiO_x$ dielectric is relatively high, but evidently it can be substantially improved by using the forming gas annealing.

The physical nature of surface states at the high $-k$ dielectric – semiconductor interface is still being debated. In addition to silicon dangling bonds, oxygen vacancy inside the high $-k$ oxide, isolated metal atom in the interlayer, or the metal atom bonded to silicon substrate can also make a contribution to the measured interface state density [4]. But the energy position of peaks in the interface state distribution and similarity of the spectra for different high $-k$ oxides allow to make a conclusion that the main defects responsible for

formation of electrically active states at the interface are silicon dangling bonds. Slight differences in position and broadening of the experimental distributions as compared to the theoretical line for a monoenergetic level is explained by variations in defect bond angles and by the presence of strain at the interface.

5. Conclusions

Thus, it was shown that the conventional *C*-*V* and *G*-ω techniques can be modified for account of a leakage current through the dielectric layer and then successfully used for the measurement of the interface state distribution in high $-k$ dielectric – semiconductor systems. Features of the interface state spectra for different high $-k$ compounds, including transition metal and rare earth metal oxides, ternary oxide $LaLuO_3$ and rare earth metal silicate $LaSiO_x$, prove that the electrically active states at the interface between dielectric and semiconductor are mainly due to silicon dangling bonds.

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References

1. J. Robertson, Interfaces and defects of high $-k$ oxides on silicon // *Solid-State Electronics,* **49**, p. 283-293 (2005).
2. H. Wong, H. Iwai, On the scaling issues and high $-k$ replacement of ultrathin gate dielectrics for nanoscale MOS transistors // *Microelectronic Eng.* **83**, p. 1867-1904 (2006).
3. O. Engström, B. Raeissi, S. Hall, O. Buiu, M.C. Lemme, H.D.B. Gottlob, P.K. Hurley, and K. Cherkaoui, Navigation aids in the search for future high $-k$ dielectrics: Physical and electrical trends // *Solid-State Electronics,* **51**, p. 622-626 (2007).
4. P.K. Hurley, K. Cherkaoui, E. O'Connor, M.C. Lemme, H.D.B. Gottlob, M. Schmidt, S. Hall, Y. Lu, O. Buiu, B. Raeissi, J. Piscator, O. Engström, and S.B. Newcomb, Interface defects in HfO_2, $LaSiO_x$, and Gd_2O_3 high $-k$ /metal-gate structures on silicon // *J. Electrochem. Soc.* **155**, p. G13-G20 (2008).
5. A. Laha, H.J. Osten, A. Fissel, Influence of interface layer composition on the electrical properties of epitaxial Gd_2O_3 thin films for high $-k$ application // *Appl. Phys. Lett*. **90**, 113508 (2007).
6. H.J. Osten, D. Kühne, A. Laha, M. Czernohorsky, E. Bugiel, and A. Fissel, Integration of functional epitaxial oxides into silicon: From high $-k$ application to nanostructures // *J. Vac. Sci. Technol. B*, **25**, p. 1039-1043 (2007).
7. A. Laha, E. Bugiel, H.J. Osten, and A. Fissel, Crystalline ternary rare earth oxide with capacitance equivalent thickness below 1 nm for high $-k$ application // *Appl. Phys. Lett*. **88**, 172107 (2006).
8. B. Raeissi, J. Piscator, O. Engström, S. Hall, O. Buiu, M.C. Lemme, H.D.B. Gottlob, P.K. Hurley, K. Cherkaoui, and H.J. Osten, High-*k*-oxide/silicon interfaces characterized by capacitance frequency spectroscopy // *Solid-State Electronics* **52**, p. 1274-1279 (2008).
9. J. Piscator, B. Raeissi, and O. Engström, The conductance method in a bottom-up approach applied on hafnium oxide/silicon interfaces // *Appl. Phys. Lett*. **94**, 213507 (2009).
10. J. Piscator, B. Raeissi, and O. Engström, Multiparameter admittance spectroscopy for metal-oxide-semiconductor systems // *J. Appl. Phys.* **106**, 054510 (2009).
11. W.K. Henson, K.Z. Ahmed, E.M. Vogel, J.R. Hauser, J.J. Wortman, R.D. Venables, M. Xu, and D. Venables, Estimating oxide thickness of tunnel oxides down to 1.4 nm using conventional capacitance–voltage measurements on MOS capacitors // *IEEE Electron Device Lett.* **20**, p. 179-181 (1999).
12. E.M. Vogel, W.K. Henson, C.A. Richter, and J.S. Suehle, Limitations of conductance to the measurement of the interface state density of MOS capacitors with tunneling gate dielectrics // *IEEE Trans. Electron Devices* **47**, p. 601-608 (2000).
13. K.J. Yang and C. Hu, MOS capacitance measurements for high-leakage thin dielectrics // *IEEE Trans. Electron Devices,* **46**, p. 1500-1501 (1999).
14. E.H. Nicollian and A. Goetzberger, MOS conductance technique for measuring surface state parameters // *Appl. Phys. Lett.* **7**, p. 216-219 (1965).
15. E.H. Nicollian, J.R. Brews, *MOS Physics and Technology*. New York, Wiley, 1982.
16. Y. Gomeniuk, A. Nazarov, Ya. Vovk, Yi Lu, O. Buiu, S. Hall, J.K. Efavi, M.C. Lemme, Low-temperature conductance measurements of surface states in HfO_2-Si structures with different gate materials // *Mat. Sci. in Semicond. Processing,* **9**, p. 980-984 (2006).
17. T. Walter, R. Herberholz, C. Müller, and H.W. Schock, Determination of defect distributions

from admittance measurements and application to Cu(In,Ga)Se_2 based heterojunctions // *J. Appl. Phys*. **80**, p. 4411-4420 (1996).

18. C.R. Helms, and E.H. Poindexter, The silicon-silicon dioxide system: Its microstructure and imperfections // *Repts Progr. Phys*. **57**, p. 791-852 (1994).
19. A. Goetzberger, E. Klausmann, and M.J. Schulz, Interface states on semiconductor/insulator surfaces // *CRC Crit. Rev. Solid State Sci*. **6**, p. 1-43 (1976).
20. G.J. Gerardi, E.H. Poindexter, P.J. Caplan, and N.M. Johnson, Interface traps and P_b centers in oxidized (100) silicon wafers // *Appl. Phys. Lett.* **49**, p. 348-350 (1986).
21. P.V. Gray and D.M. Brown, Density of SiO_2-Si interface states // *Appl. Phys. Lett*. **8**, p. 31-33 (1966).
22. Y.Y. Gomeniuk, Y.V. Gomeniuk, A.N. Nazarov, P.K. Hurley, K. Cherkaoui, S. Monaghan, P.E. Hellström, H.D.B. Gottlob, J. Schubert, J.M.J. Lopes, Electrical properties of high $-k$ $LaLuO_3$ gate oxide for SOI MOSFETs. In: Nanoscaled Semiconductor-on-Insulator Materials, Sensors and Devices, ed. by A.N. Nazarov and J.-P. Raskin // *Adv. Mater. Res.* **276**, p. 87-93 (2011).