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SYNTHESIS OF THREE-LOOP CIRCUITS OF SEMICONDUCTOR ELECTRIC DISCHARGE INSTALLATIONS WITH RESERVOIR CAPACITOR

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It is shown that if in the three-loop circuits of the capacitors of electric discharge installations (EDI) the charge thyristor is switched on after the end of the previous reverse recharge of the capacitor to a positive voltage, then in the EDI is realized a negative voltage feedback and for the capacitor charge voltage will be satisfied the inequality $U_C \le 2U_{GDV}$. If the thyristor VT_1 is switched on before the end of the capacitor reverse recharge, it is possible to realize a controllable voltage feedback, which can be either negative or positive, depending on the voltage polarity on the capacitor at the moment of VT_1 activation. References 14, figures 4.

Key words: electric circuit, capacitor, transients, analysis, synthesis, electric discharge installation.

In most cases, the synthesis of various electric discharge installations (EDI) is limited to determining the parameters of the discharge electric circuit of their reservoir linear capacitors [1-3] or nonlinear ones [4], the features of the change in the resistance of an electro-spark [5, 6] or electro-thermal [7] process load. There was a need to take into account the features of the transient processes in the EDI circuits [9] with compulsory limitation of the duration of the discharge currents in the load [5, 8] and energy losses in the energy exchange between linear and nonlinear capacitors [1–4]. An important scientific and applied problem in the synthesis of semiconductor EDI for the volumetric electro-spark dispersion (VESD) of a layer of metallic granules in a dielectric medium between electrodes is the synthesis of electric circuits of such discharge pulse generators (DPG) that would provide to production the submicron spark-eroded powders with unique properties [10, 11].

Since at a certain level of consideration all semiconductor EDI have a structure that varies as a result of switching semiconductor keys, then practically any task of realizing a certain technological process can be reduced to the problem of algorithmic-parametric synthesis [12]. In [1, 2, 5, 9, 13] the analysis and synthesis of only two-loop electric circuits of the reservoir capacitor in EDI is carried out, including analysis and synthesis of circuits in the thyristor DPG of the installations for VESD of metal in a dielectric liquid, whose active resistance R_{load} can vary from one discharge to another one [6, 13]. The use of positive voltage feedback in such DPG can substantially increase the charge voltage of the reservoir capacitors and, accordingly, the average impulse power in the load. But at the same time, the implementation of uncontrolled positive feedback in these two-loop DPG circuits can cause an unacceptable multiple increases in voltage on capacitor terminals as the result of several interconnected charge and discharge cycles of the capacitors.

Therefore, the **aim of the work** was to synthesize a simple three-loop electrical circuit of semiconductor discharge installations, which, on the one hand, would increase the average pulse power in the load, and on the other hand would limit the voltage of the charge of their reservoir capacitors.

The target function of the synthesis was chosen an increase in the average pulse power in the load $P_{av\ load} = W_{load}/\tau_{disch}$ (where W_{load} is the energy released in load during discharge of the reservoir capacitor with a capacitance C, and τ_{disch} is the duration of discharge current).

The three-loop electric circuit of the DPG of semiconductor electric discharge installations with thyristor keys is shown in Fig. 1.

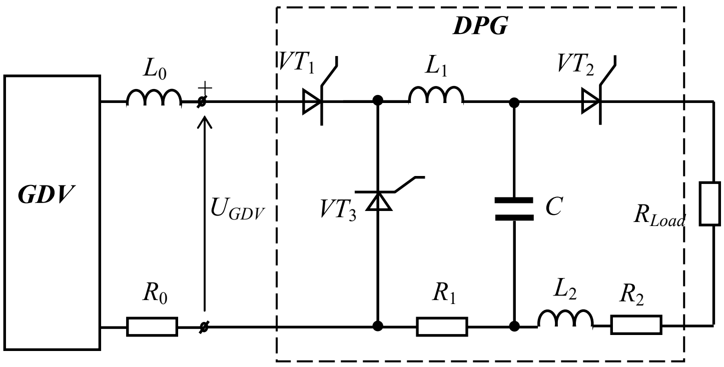


Fig. 1

The optimization criteria were the capacitor charge voltage $U_{C\ charge}$, coefficient of utilization of energy stored in capacitor $k_{util\ C} = (W_{load} + W_{R2})/W_{C\ max}$ and coefficient of efficiency of discharge circuit $\eta_2 = W_{load}/(W_{load} + W_{R2})$ (where W_{R2} – energy released at its active resistance R_2, $W_{C\ max}$ – The maximum energy accumulated in the capacitor at the initial moment of its discharge).

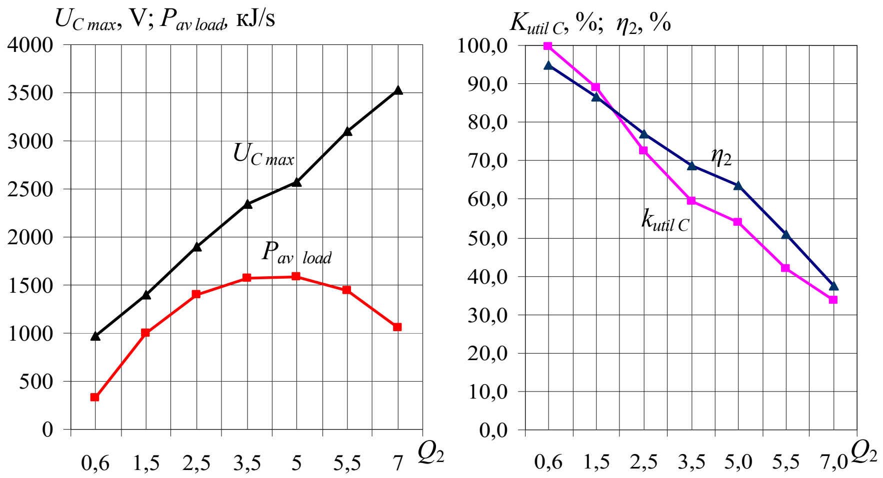
It is known that to obtain high discharge currents with high rates of their rise, it is necessary to minimize the inductance of the circuit and increase the voltage of the capacitor charge. However, technically it is difficult to realize a decrease in the inductance of the discharge circuit L_2 less than 5 μH and an increase in the charge voltage of the capacitor more than 1000 V in semiconductor DPG. Therefore, during semiconductor DPG development it is important to choose the suitable ranges of parameters of all elements.

In the calculations of the transient processes in the DPG circuits, it was taken into account that the capacitor with a capacitance $C = 10^{-4}$ F was charged from the generator of dc voltage (with $U_{GDV} = 500$ V) through a choke inductance $L_1 = 10^{-4}$ H and with a Q factor of the capacitor $Q_1 = \sqrt{L_1} \big/ R_1\sqrt{C} = 30$. The inductance of the discharge circuit of the reservoir capacitor was $L_2 = 5{\cdot}10^{-6}$ H, active resistance $R_2 = 0.02$ Ohm, and Q factor $Q_2 = \sqrt{L_2} \big/ (R_2 + R_{load})\sqrt{C}$ varies from 0.6 to 7 according to load resistance R_{load} changing.

Modeling and analysis of transient processes in the circuit in Fig. 1 were carried out using application programs MATLAB/SIMULINK. The dependences of the charge voltage of the capacitor $U_{C\,max}$ and the average pulse power in the load $P_{av\,load}$ on the Q factor of the discharge circuit Q_2 taking into account the change in its efficiency η_2 and the energy utilization factor of the capacitor $k_{util\,C}$ when the Q factor Q_2 varies from 0.6 to 7 are studied.

Fig. 2 depicts the dependences of the parameters of the DPG circuits using the positive feedback of the charge voltage of the capacitor with the value of the residual voltage at its previous discharge, on the Q factor of the discharge circuit Q_2: *a* – U_{Cmax} and $P_{av\,load}$, *b* – $k_{util\,C}$ and η_2.

Studies have shown that an increase in Q_2 leads to an increase in the voltage $U_{C\,max}$. In this case, the average pulsed power in the load $P_{av\,load}$ first increases to its maximum value (which is 4.9 times larger than the initial value of $P_{av\,load}$ at $Q_2 = 0.6$) with increasing Q-factor from 0.6 to 5 , and then $P_{av\,load}$ decreases with further increase in Q-factor (starting from $Q_2 \approx 5$). With increasing Q_2 from 0.6 to 7, the discharge circuit efficiency η_2 is reduced by 2.5 times, while the coefficient of utilization of capacitor $k_{util\,C}$ decreases by 3 times.



a ***b***

Fig. 2

It should be noted that this parametric synthesis of the electrical circuits of the dual-circuit DPG takes into account the limitations imposed on the parameters of the circuit elements and the fact that the positive voltage feedback in such a DPG is uncontrollable, that is, such feedback is not able to control the charge voltage of the capacitor $U_{C\,max}$ less then the values unacceptable for modern semiconductor switches at stochastic changes in load resistance R_{load}.

At the same time, the introduction of the third thyristor key VT_3, which is switched on after the end of the oscillatory discharge of the capacitor C to the load, makes it possible to perform an reverse oscillatory recharge of this capacitor through a choke inductance of $L_1 = 10^{-4}$ H at Q factor of the reverse-recharge circuit $Q_1 \approx 30$. If the next connection of the thyristor VT_1 occurs after the end of recharging the capacitor to the positive voltage with respect to the GDV voltage, then a negative voltage feedback will occur in the three-loop DPG circuit. This feedback will limit the voltage of the subsequent charge of the capacitor to the values $U_C \le 2U_{GDV}$. If the thyristor VT_1 is turned on until the end of the capacitor recharge, then a controllable voltage feedback, which can be either negative or positive, depending on the polarity of the capacitor voltage at the moment of switching on the thyristor VT_1, will be carry out in the DPG. In this case, it can be satisfied inequalities both $U_C \le 2U_{GDV}$ and $U_C > 2U_{GDV}$ (detailed consideration of the control laws for the turn-on time of the thyristor VT_1 after the connection of the reverse-recharge thyristor VT_3 will be presented in the following papers).

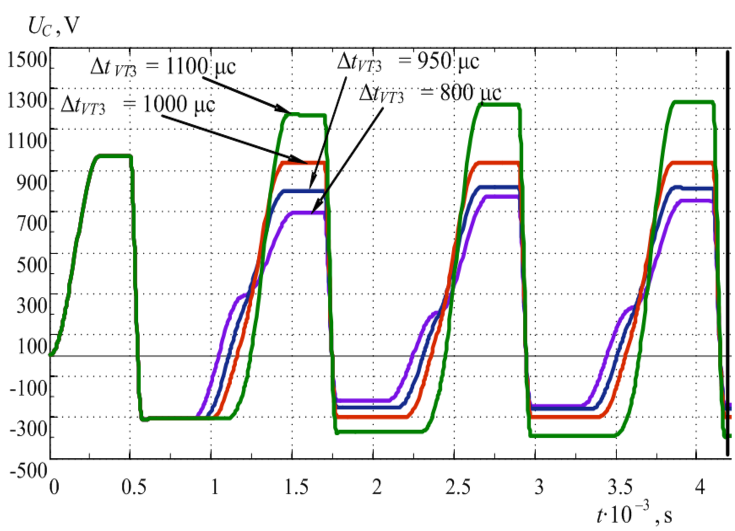


Fig. 3

Simulation of transients in the circuit shown in Fig. 1, performed using application programs MATLAB/ SIMULINK/SPS (Personal licence's password 16-11194-26164-52495-54221-19414). Fig. 3 shows the voltage oscillograms of the capacitor when the quality factor discharge circuit Q_2 = 1.5 (respectively at R_{load} = 0.13 Ohm). The repetition period of the control signals for all thyristor switches (VT_1, VT_2 and VT_3) was set identical and equal to 1200 μs and moment of turn on VT_3 (after turn on VT_1 i.e. time pause Δt_{VT3}) is varied from 800 до 1100 μs.

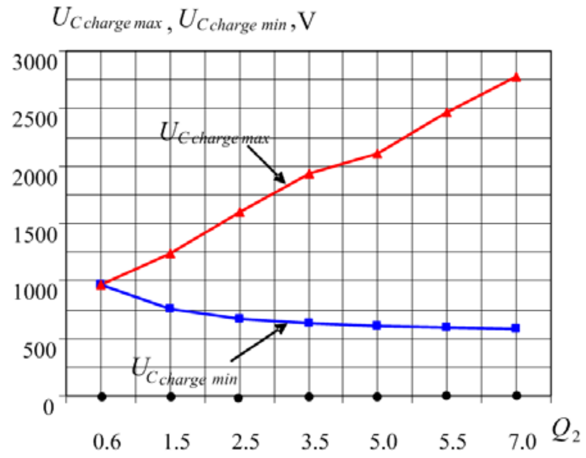


Fig. 4

As can be seen from fig. 3 the later thyristor VT_3 is switched on in the circuit of a reverse capacitor recharge (at invariable parameters of all circuits), the charge capacitor voltage is higher. Calculations show that capacitor charge voltage can be increased in 1.08 – 1.6 times by varying of delay time of turning on VT_3. The dependences of capacitor charge voltage $U_{C\,charge}$ on temporary pause Δt_{VT3}, changed from 800 to 1100 μs and on Q-factor of discharge circuit Q_2 increased from 0.6 to 7 (at the expense of decrease of resistance R_{load} at invariable resistance R_2) are defined. The influence of a temporary pause Δt_{VT3} and Q-factor Q_2 on voltage $U_{C\,charge}$ variation from the minimum value $U_{C\,charge\,min}$ to the maximum value $U_{C\,charge\,max}$ is studied too. Fig. 4 represents the variation ranges of maximum ($U_{C\,charge\,max}$) and minimum ($U_{C\,charge\,min}$) charge voltage of the capacitor (accordingly at the maximum and minimum temporary pause Δt_{VT}) as a function of Q-factor of discharge circuit Q_2.

Analysis of the results presented in Fig. 3 shows that the variation range of charge voltage of capacitor $U_{C\,charge}$ depends not only on switching time of the thyristor VT_3 for reverse recharge of capacitor, but also on a Q-factor of discharge circuit Q_2. It is determined that at invariable parameters of circuit elements the increase of a temporary pause Δt_{VT3} from 800 to 1100 μs can increase a voltage of next capacitor charge in 1,1 – 4.8 times. In this case the maximal charge voltages of the capacitor correspond to the highest value Δt_{VT3}, and minimal voltages – the smallest value Δt_{VT3}. The control range of capacitor charge voltage $U_{C\,charge}$ (from $U_{C\,charge\,min}$ to $U_{C\,charge\,max}$) is extended with increase of Q-factor Q_2: for example at $Q_2 \approx 7$ this voltage range is 4.6 times wider then at $Q_2 \approx 1.5$.

Conclusions. 1. The parametric synthesis of the three-loop thyristor DPG capacitor circuits has shown that the use of positive voltage feedback in such DPG makes it possible to increase the average pulse power in the load, but requires the introduction of restrictions because of a possible unacceptable increase in the charge voltage of the capacitor.

2. As a result of the parametric optimization performed, it is determined that the Q factor of the discharge circuit Q_2 should be changed from 1.5 to 2.5. In this case, the voltage of the charge of the capacitor $U_{C\,charge}$ can be controlled from 1.5 U_{GDV} to 3.2 U_{GDV}, and the average impulse power in the load $P_{av\,load}$ can be increased approximately by 3 times (in comparison with the modes without feedback) at sufficiently high values both of the efficiency of the discharge circuit $\eta_2 \approx 77 – 87\%$ and coefficient of utilization of energy stored in capacitor $k_{util\,C} \approx 75–89\%$.

3. If the connection of the charge thyristor VT_1 is carried out after the end of the previous capacitor reverse recharge to a positive voltage, then a negative voltage feedback will be realized in the EDI circuit shown in Fig. 1. At such feedback the inequality $U_C \leq 2U_{GDV}$ will be satisfied for the capacitor charge voltage. If the thyristor VT_1 is turned on until the end of the capacitor recharge, then a controllable voltage feedback, which can be either negative or positive, depending on the polarity of the capacitor voltage at the moment of switching on the thyristor VT_1, will be implemented.

4. Controllable voltage feedback in three-loop thyristor GDP allows to realize the wide-range control of capacitor charge voltage $U_{C\,max}$ without exceeding of allowable voltage values for modern thyristor keys. Such control is based on change in moment of activation of thyristor VT_3 in the circuit of reverse recharge of capacitor.

5. It is proved that the control range of the capacitor charge voltage depends not only on the time of activation of the thyristor for reverse recharge the capacitor, but also on the Q- factor of discharge circuit (the it is higher, the control range is wider). In order to implement of energy efficient modes of EDU, which used controllable (positive and negative) feedback, it is expedient that the Q factor of the discharge circuit is not higher than 1.5. At higher Q factor of discharge circuit its efficiency and use factor of capacitor $k_{use\,C}$ are decreased.

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СИНТЕЗ ТРИКОНТУРНИХ КІЛ НАПІВПРОВІДНИКОВИХ ЕЛЕКТРОРОЗРЯДНИХ УСТАНОВОК З НАКОПИЧУВАЛЬНИМ КОНДЕНСАТОРОМ

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Показано, що якщо в триконтурних колах конденсаторів електророзрядних установок (ЕРУ) вмикання зарядного тиристора здійснювати після закінчення попереднього перезаряду конденсатора до позитивної напруги, то в схемі ЕРУ можна реалізувати негативний зворотний зв'язок за напругою, й для напруги заряду конденсатора буде виконуватися нерівність $U_C \leq 2U_{ФПН}$. *Якщо ж вмикання тиристора* VT_1 *робити до закінчення перезаряду конденсатора, то можна реалізувати регульований зворотний зв'язок за напругою, який може бути негативний або позитивний залежно від знака напруги на зарядному конденсаторі в момент його вмикання.* Бібл. 14, рис. 4.

Ключові слова: електричне коло, конденсатор, перехідні процеси, аналіз, синтез, електророзрядна установка.

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СИНТЕЗ ТРЕХКОНТУРНЫХ ЦЕПЕЙ ПОЛУПРОВОДНИКОВЫХ ЭЛЕКТРОРАЗРЯДНЫХ УСТАНОВОК С НАКОПИТЕЛЬНЫМ КОНДЕНСАТОРОМ

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Показано, что если в трехконтурных цепях конденсаторов электроразрядных установок (ЭРУ) включение зарядного тиристора осуществлять после окончания предшествующего перезаряда конденсатора до положительного напряжения, то в схеме ЭРУ возможно реализовать отрицательную обратную связь по напряжению, и для напряжения заряда конденсатора будет выполняться неравенство $U_C \leq 2U_{ФПН}$. *Если же включение тиристора* VT_1 *проводить до окончания перезаряда конденсатора, то можно реализовать регулируемую обратную связь по напряжению, которая может быть отрицательной или положительной в зависимости от знака напряжения на зарядном конденсаторе в момент его включения.* Библ. 14, рис. 4.

Ключевые слова: электрическая цепь, конденсатор, переходные процессы, анализ, синтез, электроразрядная установка.

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