Запропонований метод лічби у кодах Фібоначчі з мінімальною формою представлення і надана його модель в вигляді набора логічних операцій, що ведуть до фібоначчієвої лічби. На цій основі був розроблений метод оптимального синтезу лічильників Фібоначчі з мінімальною формою відповідно до умов його роботи. Надана оцінка завадостійкості лічильників Фібоначчі з мінімальною формою

Ключові слова: фібоначчієві числа, мінімальна форма, лічильники Фібоначчі, завадостійкість, швидкодія

Предложен метод счета в кодах Фибоначчи с минимальной формой представления и дана его модель в виде набора логических операций, приводящих к фибоначчиевому счету. На этой основе разработан метод оптимального синтеза счетчиков Фибоначчи с минимальной формой применительно к условиям их работы. Дана оценка помехоустойчивости счетчиков Фибоначчи с минимальной формой

Ключевые слова: фибоначчиевые числа, минимальная форма, счетчики Фибоначчи, помехоустойчивость, быстродействие

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OPTIMAL SYNTHESIS OF DIGITAL COUNTERS IN THE FIBONACCI CODES WITH THE MINIMAL FORM OF REPRESENTATION

O. Borysenko
Doctor of Technical Sciences, Professor*
E-mail: 5352008@ukr.net
S. Matsenko
Candidate of Technical Sciences,
Engineer of the First Category*
I. Kulyk
Candidate of Technical Sciences, Assistant Professor*
O. Berezhna
Candidate of Technical Sciences, Assistant Professor*
E-mail: info@ekt.sumdu.edu.ua
O. Matsenko
Candidate of EconomicSciences, Assistant Professor**
E-mail: amatsenko@econ.sumdu.edu.ua
*Department of Electronics and Computer Technics
Department of Economics and Business Administration*
***Sumy State University
Rimskiy-Korsakova str., 2, Sumy, Ukraine, 40007

1. Introduction

On the agenda today, as well as earlier, there is a relevant task of increasing the speed of performance and the level of noise immunity of digital devices, which provide transfer, processing and conversion of information. The efficiency of their performance depends largely on the systems of coding, selected for them, which are the base of their work, since they, in particular, determine the structures of digital devices and their characteristics.

As a rule, an increase in the noise immunity of digital devices is accomplished based on the information redundancy, including natural, embedded in the structures of the codes they use. Noise immunity to digital devices can also be provided by noise-immune positional number systems, used for their construction, due to availability of information redundancy in them. They include such number system as binomial or Fibonacci. The peculiarity of the latter is the binary coding of their numbers. The noise-immune number systems also include a number of the multivalued number systems, such, for example, as factorial, which are implemented for the formation of permutations [1]. These and other, similar to them, noise-immune number systems are widely used for the solutions of applied problems, in particular, combinatorial optimization. Their full classification is given in [2]. In contrast to the noise-immune systems, binary, decimal and other, similar to them, usual number systems do not possess information redundancy. But they have simple structure, which simplifies their fulfillment of arithmetical and logical operations. Especially distinguished by its simplicity is the binary number system, which, due to it, is so wide-spread today in the practice for developing digital devices and systems.

In some cases, the number systems with information redundancy, in addition to providing noise immunity to the digital devices that use it, increase their performance speed while solving a number of special problems. As a result, there appears a possibility for the digital systems, which use such devices, to achieve, in the same codes, a start-to-finish control of information processing and transmission. Their efficiency thus considerably increases both from the point of view of the control of errors in the data processed by them, and the speed of their processing. In this case, a required amount of hardware expenses can be reduced, which, in its turn, leads to the improved reliability of the systems. A useful feature of digital devices, which function in the noise-immune number systems, is also the fact that the redundancy in them, necessary for detection of errors, is evenly distributed in the structures of their schemes, which gives them homogeneity, and, therefore, technological efficiency of their

manufacturing. Furthermore, the control schemes of digital devices in such number systems, as a rule, require minimum quantity of hardware expenses for their realization, and the digital devices themselves acquire increased reliability.

Among the noise-immune number systems, the Fibonacci number systems, which work in Fibonacci codes, which are the sets of the Fibonacci numbers, have in the recent decades gained special importance, owing to their simplicity. They use, for representations of numbers as the weight coefficients, the Fibonacci numbers. Their theory began active development from the beginning of the sixties of the past century, after writing a paper on the Fibonacci numbers [3]. The book "Fibonacci & Lucas Numbers, and the Golden Section. Theory and Applications" was published in 1989 [3]. It developed and expanded the ideas, presented in the work [3], on the Lucas numbers and the area of golden section and conducted their study. There were other works on this topic, for example, the paper [5]. It thoroughly examined, for the first time, the minimal and maximal form of representation of the Fibonacci codes. The given and other similar papers laid the foundation for the theory of the Fibonacci numbers.

In the seventies of the past century, based on these books, the theory of the noise-immune codes of Fibonacci was proposed, and the idea was put forward of developing "the Fibonacci computers" based on them, partially realized in the papers [6, 7]. Initially this idea attracted many supporters; however, later on, in connection with the explosion of computer technology based on the binary number system, interest in the Fibonacci computers decreased, though, in spite of this, it still exists.

Most likely, should the universal Fibonacci computers appear, then this does not happen any time soon, while the various existing Fibonacci digital devices, described, among others, in the papers [6, 7], can be effectively utilized today. The devices of digital Fibonacci calculation, the Fibonacci pulse counters, are of special importance among them. Due to their possibility of detecting errors, they are capable of increasing their noise immunity. Furthermore, the Fibonacci counters make it possible to speed up their performance during calculation owing to the absence of carries between the bits.

The Fibonacci counters can be effectively used also for constructing coding and decoding devices that makes it possible to build on their basis noise-immune communication networks in the Fibonacci codes. A start-to-finish control is possible in them, both at transmitting information and at its processing, which can considerably increase their efficiency. Positive effect in this case is achieved due to the use of the same codes both for the control of digital devices that process information and for the control of communication channels. This reduces hardware expenses, required for the work of a network, and increases its performance speed and reliability.

2. Literature review and problem statement

Counters are the most common devices of digital technology because not a single contemporary digital device is possible without them, starting from the sensors of various specialized devices and systems and ending with computers and their systems. However, binary counters in the known schemes, for increasing their performance speed, used those methods that required considerable hardware expenses, which decreased reliability of their performance. More to the point, the counters' structures turned more complex, which disrupted the homogeneity of their structure while decreasing their manufacturability. Thus, in the patent [8], an attempt at increasing operating speed of the counter required the increase in the hardware expenses, which, in turn, decreased its reliability but raised the cost. Sufficient measures to boost its noise immunity were not undertaken either.

The article [9] proposes binary composite counters with the selective carry (Carry-Select Counters), whose performance speed is quite close in value to the counters with parallel operation. However, the amount of the necessary hardware expenses proved to be too large. There were also practically no schemes, which protected the counter from the noises, which, with an increase in speed, tend to grow. Additional shortcoming of the counters, given in the paper [9], is impossibility to read the data immediately after the end of calculation, which complicates compatibility of such computing devices with other digital devices.

The articles [10, 11] describe the binary counters, the high switching rate of which is reached due to realization of the capacity to preset their subsequent states. This ability is defined by the authors as "Pipeline Partitioning". An essential drawback of such counters is a relatively large number of logic elements that organize connections between the bits, which leads to noticeable hardware expenses and increase in the transfer time of count signals.

A characteristic shortcoming of all the devices described above is the presence of carries, which slows their work, and the capacity to control errors. These shortcomings are successfully removed by the Fibonacci counters that use the Fibonacci codes. They make it possible to optimally combine hardware expenses, performance speed and noise immunity. However, even here the results proved to be rather inefficient because of the necessity of transfer from the minimal form to the maximal form of representations of the Fibonacci numbers and back with the help of operations of convolutions and deconvolutions, as this was proposed to carry out in the papers [12–14]. But the evaluation of performance speed and noise immunity of the proposed Fibonacci counters was not performed up to the level in these articles. Although it is obvious that their performance speed, because of the absence of carries, is higher than that of the binary counters at the same hardware expenses. They are also characterized, along with the noise immunity, by increased performance reliability. Therefore, they are promising for practical purposes from this point of view. However, the presence of operations of convolution and deconvolution in their work is also their drawback, which decreases both the performance speed and noise immunity.

That is why the task was set of the synthesis of high-speed Fibonacci counters, which work only in the minimal form and do not use operations of convolution and deconvolution. Such a counter was for the first time synthesized in [15]. But it was not optimal from the point of view of speed performance, hardware expenses and noise immunity under all possible conditions of its work. That is why the task was set of the synthesis in connection with the specific conditions of the work of Fibonacci counters with the optimum structure in the minimal form. This particular problem is being solved in this work.

3. The purpose and objectives of the study

The purpose of this work is to increase performance speed and noise immunity of digital pulse counters.

To achieve the set goal, two problems are being solved:

– to develop a universal method of synthesis of the Fibonacci counters, which work in the minimal form;

– to carry out assessment of the noise immunity of the Fibonacci counters, synthesized by the proposed method.

The estimation of performance speed and hardware expenses is solved for each structure of the Fibonacci counter separately after its synthesis and, therefore, it is beyond the scope of the stated purpose.

4. Materials and methods of studies of the Fibonacci codes

By the Fibonacci codes we understood the sets of the Fibonacci numbers, which used, as the weight coefficients of their bits, the Fibonacci numbers, included in the Fibonacci sequence – 0, 1, 1, 2, 3, 5, 8, ..., F_n. Each number in it, starting from the third one, is determined as the sum of the two preceding numbers [7]. This condition corresponds to the recurrent ratio:

$$F_n = F_{n-1} + F_{n-2}. \quad (1)$$

However, at formation of the Fibonacci codes, only the part of the Fibonacci sequence 1, 2, 3, 5, 8, ..., F_n is usually used. Zero in this case is excluded.

A non-negative integer Fibonacci number in the minimal form is represented by the following numerical (numbering) function [6]:

$$N = a_n F_n + a_{n-1} F_{n-1} + ... + a_i F_i + ... + a_1 F_1, \quad (2)$$

$$F_1 = 1,\ F_2 = 2.$$

Its abbreviated record takes the form: $N = a_n a_{n-1} ... a_i ... a_1$, where $a_i \in \{0,1\}$ is the binary digit of the i-th bit of the positional representation of the number (2); n is the code bit capacity; F_i is the weight of the i-th bit, which equals the i-th Fibonacci number. For example, the Fibonacci number is 10101=1·8+0·5+1·3+0·2+1·1=12.

From the onset of appearance of the Fibonacci codes, two forms of their representation of the Fibonacci numbers, included in them, were examined – minimal, which is also called normal, and maximal. They seem to complement each other because they make it possible to perform arithmetic operations, passing, with the aid of special operations of convolutions and deconvolutions, from the minimal form to the maximal form and back. However, this approach of performing arithmetic operations caused certain inconveniences while constructing the Fibonacci counters, due to the increase in the complexity of their design and decrease in the speed of performance. That is why the idea came up to use, for synthesis of the counters, only minimal form of representation of the Fibonacci codes without their transfer to the maximal form and back.

The minimal form of the representation of the Fibonacci codes is main for them. That is why, at first, the Fibonacci numbers were represented in this form [3]. The Fibonacci numbers were used as the weights of digits in their bits. Table 1 demonstrates an example of the Fibonacci code in the minimal form, whose numbers emerge from the series of the Fibonacci numbers 1, 2, 3, 5. They differ in the table from each other by 1. The range of the Fibonacci numbers is equal to the sum of the weights of the high-order and low-order bit of the Fibonacci number, adjacent to it – 3+5=8.

Table 1

Fibonacci code in the minimal form

Bit number	4	3	2	1
Bit weight	5	3	2	1
Digit of the i-th bit	a_4	a_3	a_2	a_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	0	1	0	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0

The minimal form of the Fibonacci code takes the form 100, and the maximal – 011. It is possible to pass from the minimal form of the Fibonacci code to its maximal form and back after performing operations of convolution and deconvolution. They take the form, respectively, – 100→011 and 011→100. This means that the Fibonacci number in the minimal form 100 can be represented as 011 in the maximal form. The quantitative equivalent of the Fibonacci number in the maximal form 011 coincides with the quantitative equivalent of the Fibonacci number 100 in the minimal form and back. For example, if the weights of the low-order two digits of the number in the maximal form, where there are ones, are equal to 3 and 5, then their sum will equal 8, which corresponds to the weight 1 of the corresponding number in the minimal form and, therefore, the Fibonacci numbers 011 and 100 by the weight equivalent are equal to each other 011=100=8. It should be noted that convolutions and deconvolutions simplify fulfillment of arithmetic operations and that is why they are widely used for constructing the Fibonacci arithmetic, composing its basis. Its special case, the Fibonacci calculation, is widely used for constructing the Fibonacci counters [6, 7].

5. Main properties of the Fibonacci codes in the minimal form

Among many known properties of the Fibonacci codes in the minimal form, we will highlight the following properties, most frequently used in practical problems [6, 7].

1. The Fibonacci number, in which ones are in all odd bits 1, 3,..., n, represents the largest possible number among all Fibonacci numbers of odd length n and equals $F_{n+1} - 1$. Such a five-digit Fibonacci number is the number 10101=8+0+3+0+1=12.

2. The Fibonacci number, in which ones are in all even bits 1, 2, ..., n, represents the largest number among the Fibonacci numbers of even length n and equals $F_{n-1} - 1$. Thus, the Fibonacci four-digit number 1010=5+0+2+0=7 will be maximal among all Fibonacci numbers of the same length.

3. The number (range) of the Fibonacci numbers of length n equals $P = F_{n+1} = F_n + F_{n-1}$.

For example, a quantity of the Fibonacci numbers of length 5 in the Fibonacci code is equal to the sum of the weights of the elder 5th and adjacent to it 4th low-order bits – 8+5=13. At the length of the Fibonacci numbers equal to 4 digits, their number in the Fibonacci code equals 5+3=8. All of them are represented in Table 1.

4. In the minimal form of the Fibonacci code, appearance of two ones in a row is forbidden.

This particular property makes the Fibonacci numbers in the minimal form noise-immune. We will note that Table 1 does not contain any Fibonacci number, in which two ones are next to each other.

Unique property, poorly explored as yet, of the Fibonacci codes is the fact that fulfillment of arithmetic operations within them does not require the carries between the bits of their numbers, which indicates potential possibility of constructing high-speed schemes of the Fibonacci calculation.

6. Study of the noise immunity of the Fibonacci counters with the minimal form of representation

A shortcoming in the Fibonacci numbers in the minimal form is the fact that they reveal only erroneous transfers of 0 to 1, and the transfers of 1 to 0 are not revealed. But the quantity of zeros in the Fibonacci numbers exceeds the quantity of ones by times, and that is why, even in the symmetrical communication channels, erroneous transfers of zeros to ones will predominate over those of ones to zeros. This enables us to speak about acceptable immunity of the Fibonacci code in the minimal form from the errors. However, in the real digital schemes, the errors are asymmetrical and that is why such a coding of the Fibonacci numbers with the minimal form can reveal the majority of their errors. This means that the Fibonacci codes by their structure are adapted for detecting errors in digital schemes, which by their nature model asymmetrical communication channels.

Errors in the Fibonacci numbers, as in any other codes, can be detected and corrected only when their transfer occurs to the forbidden combinations, and the more forbidden combinations in the code, the higher its noise immunity will be. That is why an important stage in the study of any noise-immune code is determining the number of permitted and forbidden code combinations in it. As was indicated above, for the Fibonacci numbers with the minimal form, appearance of two and more 1 next to each other is forbidden, which is equivalent to the ban of appearance of at least one 0 between the ones next to each other in the number [6, 7]. The violation of this ban testifies to the presence of errors in the Fibonacci numbers. That is why such numbers relate to the forbidden code combinations, whose number together with the permitted Fibonacci numbers equals 2^n. Since the appearance of several, standing next to each other, ones usually occurs in the error packets, then the Fibonacci code is capable to detect them first of all. But single errors are also easily detected with its aid.

For the example of the Fibonacci code, examined above in Table 1, which consists of 8 permitted 4-digit Fibonacci numbers, there will be 8 forbidden code combinations. For example, such combinations are 0011 and 0110. The number of forbidden combinations is determined by the difference $2^n - P = 2^n - (F_n + F_{n-1})$. Each of them contains at least 2 ones next to each other. That is why appearance of any of these numbers is the error. The larger the number of forbidden combinations relative to the number of those permitted, the higher is the capacity to reveal errors in the code.

For estimation of the efficiency of application of the Fibonacci numbers, it is at first necessary to solve the task of determining the share of the detected errors, and then the share of the errors not detected. In the first case, this will be the ratio of the number of permitted combinations to their total number, and in the second – ratio of forbidden combinations to this number. These shares are the probabilities of appearance of the forbidden and permitted combinations at equal probability of appearance of all possible combinations. They characterize directly the codes without taking into account parameters of the communication channels, thus representing universal characteristics of these particular codes.

The share of the detected errors is determined by the known formula [6]:

$$D = 1 - \frac{P}{N}, \tag{3}$$

where P is the number of permitted code combinations – the Fibonacci numbers; N is the number of all possible combinations of the assigned length n.

After substituting the values of magnitude P into the formula (3) and accepting $N=2^n$, it is possible to obtain the share of the detected errors in the Fibonacci numbers for each value n=1, 2, ...

$$D = 1 - \frac{F_n + F_{n-1}}{2^n}. \tag{4}$$

It is obvious that for n=1 the forbidden combinations are absent because the Fibonacci code degenerates into two permitted code combinations – 0 and 1.

Fig. 1 presents, in the form of a solid line, the chart that shows the share of the detected errors depending on the bit capacity n=5 of the Fibonacci numbers. A dotted line shows the graph, which reflects the share of the errors, not detected, for the same bit capacity of the Fibonacci numbers n=5. It is obvious that the share of the detected and the share of those not detected errors give 1 in the sum, forming a full group of probabilities.

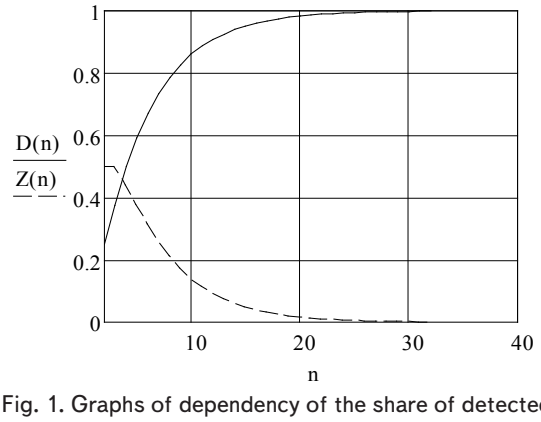

Fig. 1. Graphs of dependency of the share of detected and those not detected errors on the bit capacity n of the Fibonacci codes

It follows from the graphs in Fig. 1 that the share of the detected errors D in the Fibonacci code grows with an

increase in n and it seeks to limit to one while the share of the errors Z, not detected, in this case is approaching zero. The conclusion follows that the larger the length of the Fibonacci numbers, the higher is their capacity to detect the errors. That is why the Fibonacci counters with the larger bit capacity are more efficient from the point of view of noise immunity in comparison to the counters with small bit capacity. This is one of the reasons why it is expedient to design the multidigit Fibonacci counters rather than compile them from the counters with small bit capacity.

7. Logical model of Fibonacci counters with the minimal form of the representation

In the Fibonacci counters with the minimal form of representation, the capacity of significant increase in performance speed and natural noise immunity, inherent to them, are combined. The increase in performance speed, as already mentioned earlier, is the result of absence of the carries of ones at calculation. This is explained by the specific character of Fibonacci calculation and by the absence of operations of convolutions and deconvolutions. Noise immunity is explained by the availability of forbidden states in the Fibonacci counters. Two or more ones next to each other correspond to them in the Fibonacci numbers.

The attempt to exclude from the operations of calculation the carry of operations of convolutions and deconvolutions led in its time to the method of the Fibonacci calculation with the minimal form of representation of the Fibonacci numbers. The idea of this method is the presence of two zeros in the Fibonacci number, represented in the minimal form. They are located at the look at the digits of the Fibonacci number from right to left. After this, the transition is performed of the first of zeros that is on the right, to 1. Simultaneously occurring is the transition of the values of all low-order digits, which are before this zero, to zero. The Fibonacci number, next on order, is obtained.

For example, if the 8-digit Fibonacci number is assigned in the minimal (normal) form 01000101 with the weights 1, 2, 3, 5, 8, 13, 21, 34, equal to 25, then the next in order there will be number 01001000, equal to 21+5=26. It is received like this because, with the sequential survey of the digits of the initial number from the right, starting from the 4th bit, three zeros, next to each other, are observed. This is the signal that zero in 4 bit must be converted to 1 while all low-order digits, preceding it, including the first bit, must be converted to 0. By following the given logic, it is obvious that the next number after number 01001000 will be number 01001001 equal to 27. Number 28, obviously, will equal 01001010. By analogy, all the remaining Fibonacci numbers can be obtained, whose number for the present case equals 21+34=55. Appearance of two and more ones in the normal Fibonacci number, for example, 01100101 will be recorded as error.

This method of the Fibonacci calculation in the minimal form makes it possible to simplify realization of the Fibonacci counters both in the hardware and program form. However, it does not by itself provide another possibility to obtain different structures of the Fibonacci counters. For their synthesis, it was necessary to also develop logical model of the method of the calculation of the Fibonacci numbers in the minimal form. Subsequently, based on it, it was possible to obtain a universal method of the optimal synthesis of various variants of the Fibonacci counters with the minimal form for any bit capacity n.

Such a logical model of the Fibonacci calculation in the minimal form takes the following form:

1. In the given Fibonacci number $F = x_1, x_2, ..., x_j, ...x_n$ when calculating from right to left, 2 adjacent bits are located, the sum of which $x_j \vee x_{j-1} = 0$, j=1, 2, ... n.

2. If one will not find in the Fibonacci number the sum $x_j \vee x_{j-1} = 0$, then the calculation finishes.

3. If this sum is found, then 1 is included in the x_j bit and all the bits, which are located to the right of it, are set to 0.

4. If, in the obtained code, the composition $x_j \wedge x_{j-1} = 1$, then the received number is erroneous. Stop.

5. If the composition $x_j \wedge x_{j-1} = 0$ for all j, then the received Fibonacci number is correct.

It is obvious that this model can be used for synthesis of the Fibonacci counters both in the schematic and program variant.

8. Method of synthesis of the Fibonacci counters with the minimal form of representation

The logical model of the Fibonacci calculation in the minimal form shows that the corresponding Fibonacci counters must contain the following blocks: Register, Block of analysis of the register outputs, Block of register control, Block of setting the triggers to zero, Block of dispositions, Block of errors control. The indicated blocks make possible to reduce synthesis of the Fibonacci counters in the minimal form to two stages – synthesis of internal structures of the indicated blocks – serial, parallel, serial-to-parallel, and synthesis of particular system connections between the blocks of the counter.

The set-up and functions of each block are the following:

1. The register contains n memory elements (triggers) and is intended for storing the Fibonacci numbers. Each trigger has capability to forbid the change in the state of the trigger of high-order bit next in order to it. That is why, in the zero state of the counter, only the memory element of the first bit can be set to 1. This means that after the state 00000 the counter can transfer only to the state 00001.

2. The block of analysis contains n–1 of two-input schemes AND, each of which corresponds to two adjacent triggers. They issue single signals only in the case when the triggers, corresponding to them, are in the zero state. In the remaining cases, they issue zero signals. That is why, for example, in the state of the 5-bit Fibonacci counter of 10101, there will be signal 0 in all 4 schemes AND, which indicates the end of calculation.

3. The block of register control consists of n of the 4-input schemes AND, the output of each of which is connected to the input of setting the trigger to a single state. One of the inputs of each scheme AND is connected to the input of clock pulses. The remaining three inputs are controlling, forbidding or permitting setting the corresponding triggers to a single state and discarding in this case all memory elements of the low-order bits to a zero state. Thus, if there is the Fibonacci number 01001010, then the signal, delivered from the 5th scheme AND, will set the corresponding trigger to 1, and all 4 triggers of low-order bits – to 0. The number will be as a result obtained 01010000.

4. The block of setting the triggers to zero contains n–1 of elements OR. The output of each of them is connected to

the inputs of setting to zero of the corresponding trigger. The number of inputs of schemes AND, depending on the structure of the counter, can take the value from 2 to n. The inputs of the OR schemes are connected to the appropriate outputs of the block of register control, from their AND schemes.

5. The block of dispositions contains n–1 schemes AND with inverse inputs. The number of inputs of each of them, depending on the structure of the counter, is within the range from 2 to n. Signals from the outputs of AND schemes possess a capacity, through the appropriate AND scheme of the control block and further OR scheme of block of setting to one, to set into initial state all memory elements, preceding them.

In the synthesis of counters with the minimal and maximal performance speed, the number of inputs for all AND schemes in the first case will equal 2, and in the second – consistently growing to 2, 3 and to n.

6. The block of errors control contains n–1 of two-input AND schemes, each of which, with the exception of the first and n–1, is connected by the second input to the first input of another one and direct output of the corresponding trigger of the register. The first and second input, in line with the first and n–1 OR schemes of the control block, are connected to direct outputs of the first and the n-th the trigger of the register. The outputs of all AND schemes are connected to the OR scheme, which indicates presence of error in the counter. Signals 1 at the outputs of separate AND schemes of control block indicate two bits of the counter, corresponding to it, in one of which the error occurred.

This method of synthesis was verified in the synthesis of the counter [15]. Its workability was checked and tested with the aid of computer simulation. The result was positive. The counter confidently functioned in all verifying modes, it demonstrated high speed operation and found both the single errors in the form of transfers 0 to 1 and the packets of similar errors.

By varying connections of the blocks of the Fibonacci counter in different ways, and their elements inside the blocks, it is possible to obtain their different structures. Each of them possesses its own value of performance speed, noise immunity and hardware expenses. From this array of structures, it is possible to select the structure, which will optimally correspond to the initial requirements to the counter. As a result, it will be possible to produce the optimal synthesis of the Fibonacci counters.

9. Discussion of the results of the study of noise immunity of the Fibonacci codes

The results obtained in the work show that the Fibonacci codes with the minimal form of representation of numbers, in comparison with the usual binary counters, are capable, with high probability, of revealing the errors in their performance in the form of transfers 0 to 1. In comparison to the counters with detection of errors, they require less hardware expenses for their realization and display higher performance speed. That is why the Fibonacci counters with the minimal form are promising for constructing high speed noise-immune pulse counters.

The evaluation of the noise immunity of the Fibonacci codes in the minimal form, used in the Fibonacci counters, demonstrates good noise immunity of the counters even at small bit capacity. The share of the errors, detected in the Fibonacci codes, increases with the increase in the bit capacity of their combinations. Especially efficient are such codes in the systems with asymmetric nature of appearance of errors because errors in the Fibonacci codes are revealed only at transfers of 0 to 1.

Taking into account that the Fibonacci codes by their nature are capable of detecting errors in the Fibonacci counters and simultaneously in the communication channels, it is possible to apply them in the systems, which process and transmit information, realizing, in so doing, their start-to-finish control. Thus, the use of the high speed noise-immune Fibonacci counters with the minimal form in the systems of collection and transmission of information increases considerably the authenticity of performance of the information transmission system and simplifies its structure.

10. Conclusions

1. The characteristic feature of the method of synthesis of the high speed noise-immune Fibonacci counters with the minimal form of representation is the possibility of their optimal synthesis, based on logical model. Logical model is a set of logical operations, which ultimately lead to the structure of a synthesized counter with the set parameters by performance speed, noise immunity and hardware expenses. The proposed method differs from the known methods by the possibility of synthesis of the optimal structure of the Fibonacci counter. Especially important is the fact that, among the Fibonacci counters synthesized with the aid of this method, there is a ultra-high-speed counter, which has minimal signal delay, not depending on the bit capacity of the counter.

2. The performed evaluation of noise immunity of the Fibonacci counters with the minimal form showed their high noise immunity for asymmetric errors, which are most probable in the digital devices in general, and the Fibonacci counters in particular. With an increase in the bit capacity of the Fibonacci counters, the probability of detecting errors in them considerably increases. That is why it is expedient to use in practice multibit counters, rather than compile them from the counters with a small number of bits. It is especially important for the high speed and ultra-high-speed Fibonacci counter, for which the probability of occurrence of errors, as a result of the increase in the switching rates of their elements, considerably increases.

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Розглянуто проблему точності класифікації, яка визначається часткою правильно класифікованих об'єктів при використанні параметричних методів. Показано, що нерівність коваріаційних матриць класів приводить до зміщення поверхні, яка їх розділяє, однак це може не суттєво впливати на точність класифікації. Показано, що локалізація векторів-образів на основі планів повного факторного експерименту забезпечує можливість підвищення точності класифікації

Ключові слова: параметрична класифікація, коваріаційна матриця, розпізнавання образів, точність класифікації об'єктів, вектор-образ, кластер

Рассмотрена проблема точности классификации, определяемой долей правильно классифицированных объектов при использовании параметрических методов. Показано, что неравенство ковариационных матриц классов приводит к смещению разделяющей поверхности, однако это может не существенно влиять на точность классификации. Показано, что локализация векторов-образов на основе планов полного факторного эксперимента обеспечивает возможность повышения точности классификации

Ключевые слова: параметрическая классификация, ковариационная матрица, распознавание образов, точность классификации объектов, вектор-образ, кластер

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LOCALIZATION OF VECTORS-PATTERNS IN THE PROBLEMS OF PARAMETRIC CLASSIFICATION WITH THE PURPOSE OF INCREASING ITS ACCURACY

Mourad Aouati
Chief Commissioner of Police
Central City Police Department of Constantine
Ali Mendjeli UV 01 Ilot 03 Bt H n°123
Constantine, Algeria

1. Introduction

Solving the problems of pattern recognition, which appear in many applications, requires, mainly, an increase in the accuracy of classification that is understood in the sense of minimization of the share of incorrect classifications of objects. When such problems are solved for face recognition [1, 2], identification of objects by their text,