Удосконалена математична модель біполярного транзистора з ізольованим затвором за рахунок встановлення аналітичних виразів для динамічних паразитних ємностей приладу. Вирази знайдені шляхом аналітичного диференціювання функцій, які апроксимують залежності паразитних ємностей транзистора від напруги між колектором та емітером. Запропонована методика формування математичної моделі IGBT інвертора напруги у вигляді матричних диференційних рівнянь стану в формі Коші та нелінійних рівнянь зв'язку. Обмеження на кількість транзисторів та конфігурацію схеми відсутні. Методика базується на матрично-топологічному методі аналізу електричних кіл. Застосування методики проілюстровано на прикладі однофазного напівмостового інвертора з активним навантаженням. Актуальність удосконалення математичної моделі IGBT інвертора викликана необхідністю аналізу електробезпеки стану кола змінної частоти між частотним перетворювачів та двигуном. Відомі моделі частотно-керованих електроприводів не враховують ряд факторів, які суттєво впливають на точність моделювання. До таких факторів відносяться динамічний характер паразитних ємностей IGBT та відклю-чення однієї з фаз машини від мережі на час безструмової паузи при переми-канні суміжних силових ключів інвертора. Отримана математична модель відрізняється від відомих удосконаленим представлення нелінійними диференційними рівняннями окремих елементів та врахуванням взаємних впливів. Запропонований підхід дозволяє досліджувати високочастотні перехідні складові струмів та напруг в електротехнічних системах з напівпровідниковими перетворювачами. Це спрощує врахування в моделі процесів перезаряду ємностей IGBT під час безструмової паузи при комутації суміжних ключів. Виявлені особливості перехідних процесів комутації ключів IGBT інвертора, зокрема, встановлено суттєве, більше ніж удвічі, перевищення струмом транзистора, що відкривається, робочого рівня наприкінці процесу комутації

Ключові слова: паразитні ємності, широтно-імпульсна модуляція, матриця головних перетинів, змінні стану, дерево графа, топологічні рівняння

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IMPROVEMENT OF THE MATHEMATICAL MODEL OF SINGLE-PHASE HALF-BRIDGE INVERTER IN STATE-VARIABLE FORM

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1. Introduction

The insulated-gate bipolar transistors (IGBT) are widely used in power circuits of frequency converters for electric drives, inverters for electric cars, wind turbines, solar power plants, active filter circuits, pulsed DC converters, etc. IGBT are available for voltage up to 6,5 kV (leading manufacturers – Mitsubishi, ABB, Hitachi) and current up to 3.6 kA (for example, 5SNA 3600E170300). Increasing the efficiency and reliability of the "autonomous inverter – induction motor" system operation requires the study of transients during power switches commutations. This provides the corresponding mathematical model improvement, which takes into account the features of the semiconductor devices switching, the motor operation in nonsymmetrical modes, mutual influences of power switches and motor windings and allows to investigate emergency states.

2. Literature review and problem statement

The mathematical modeling of IGBT functioning as the part of semiconductor converters allows to analyze combined action with motor loading in normal and emergency states for selection of the rational operation modes and development of the newest protection devices. The models of IGBT, which take into account the physical principles of semiconductor operation, are known. Such models are the most complex and precise. In particular, a method for simulating IGBT with a reverse diode is proposed in [1], which involves solving the charge carrier diffusion equation using the finite differential method.

Associative models, which reproduce static and dynamic characteristics by different methods, are most often used. Such models are less complex and precise than models of the first type. In particular, in [2] IGBT with a reverse diode, in accordance with the Thévenin theorem, are represented by a voltage source. This allows to use a fixed equivalent circuit for open and closed states of the transistor. It is assumed in [3] that capacitance between IGBT leads does not depend on the voltage between the collector and the emitter, which reduces the accuracy of the transients simulation. In [4] only the static dependences of spurious capacitances from the voltage on the device are considered, the dynamic component is ignored.

Combined models that use existing models of field-effect and bipolar transistors, taking into account the specificities of IGBT operation [5], are also well-known.

During the analysis of the IGBT-inverter and motor joint action, simplified models are often used that ignore non-linearity of characteristics and transients during IGBT commutations. In particular, when modeling a multi-level inverter in [6], power switches are considered as ideal. The inverter is often represented as an ideal source of impulse voltage, or its characteristics are linearized and it is represented by a dynamic link. During the analysis of a frequency-controlled electric drive, in most cases, the motor is considered as a symmetrical load, as, for example, in [7].

Thus, known models do not take into account a number of factors that are significant for the analysis of the operation of a frequency-controlled electric drive. These factors include the dynamic nature of the IGBT spurious capacitances and the disconnection of one of the machine phases from the network during the dead time when switching adjacent power switches of the inverter. Herewith, as it is established in [8], the transition of an induction machine from a three-phase to a single-phase mode is accompanied by the appearance of current transient components of a significant magnitude. Taking these factors into account will allow to study processes of a ground fault or current leakage to ground through the resistance of the human body in the cable, by which the motor is connected to the converter. The urgency of such emergency modes study is determined by the functional deficiency of existing protective devices, which is experimentally illustrated in [9].

The consideration of the dynamic capacitances between the IGBT leads and the asymmetric motor operating modes in the mathematical model of the inverter is a variant to solve the actual problem of increasing the analysis accuracy of processes in systems equipped with semiconductor converters.

3. The aim and objectives of the study

The aim of the work is to improve the accuracy of modeling the voltage inverter by improving the model of the IGBT module and forming a mathematical model of the power part of the converter in the state variables using the example of a single-phase half-bridge inverter.

To achieve the set aim, the following objectives must be accomplished:

– to improve the dynamic IGBT model by taking into account dynamic spurious capacitances between the leads of the device;

– to form the mathematical and corresponding computer model of the inverter power part;

– to research into features of the IGBT inverter switching process, taking into account the delay between the switching of the adjacent switches.

4. Mathematical modeling of the IGBT module

Commercially available power modules include one or more IGBT, between the collector and the emitter of each of which a reverse diode is connected. The IGBT can be represented by an equivalent circuit that takes into account the family of non-linear static volt-ampere characteristics by a controlled current source I_c (Fig. 1). The variconds C_1–C_3 represented spurious capacitances between the transistor leads, which allows to take into account dynamic processes during switching [10]. Darlington's IGBT representation (BJT controlled by MOSFET) allows to determine the current of a controlled source I_c as a function of the voltage u_{CE} between the collector and emitter of IGBT [5]:

$$I_c(u_{CE}) = \begin{cases} 0, \text{if } u_2 \le u_{Th} \ \ or \ \ u_{CE} < u_D; \\ k[(u_2 - u_{Th})(u_{CE} - u_D) - 0{,}5(u_{CE} - u_D)^2], \\ \text{if } \ u_{CE} < u_2 - u_{Th} + u_D; \\ 0.5k(u_2 - u_{Th})^2, \\ \text{if } \ u_{CE} \ge u_2 - u_{Th} + u_D, \end{cases} \quad (1)$$

where $k=k_p(1+\beta)$, β – the current gain of the BJT; u_{Th} – threshold of the field transistor opening voltage; u_D – voltage drop on the emitter-base junction of BJT; u_2 – voltage between the IGBT gate and emitter.

The capacitances C_1–C_3 values between the transistor leads (Fig. 1) are related to the typical capacitances of IGBT, dependencies of which on the collector-emitter voltage are given in the data sheet, as follows:

$$C_1(u_{CE}) = C_{res}(u_{CE}); \quad (2)$$

$$C_2(u_{CE}) = C_{ies} - C_{res}(u_{CE}); \quad (3)$$

$$C_3(u_{CE}) = C_{oes}(u_{CE}) - C_{res}(u_{CE}), \quad (4)$$

where C_{ies} – the input capacitance (is measured between the gate and the short-circuited collector and emitter), the value of which can be considered to be independent of the voltage between the collector and the emitter with sufficient accuracy; $C_{res}(u_{CE})$ – capacitance between the collector and the gate with a grounded emitter; $C_{oes}(u_{CE})$ – the output capacitance, which is measured between the collector and the short-circuited gate and emitter.

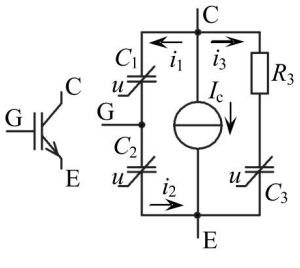

Fig. 1. The IGBT equivalent circuit:
E – emitter; *C* – collector; *G* – gate

The dependences of $C_{res}(u_{CE})$, $C_{oes}(u_{CE})$ can be approximated by the power functions of the following form [10]:

$$C_{res}(u_{CE}) = C_{resh} + C_{res0}(1 + u_{CE})^{-k_{res}}; \quad (5)$$

$$C_{oes}(u_{CE}) = C_{oesh} + C_{oes0}(1 + u_{CE})^{-k_{oes}}. \quad (6)$$

Since the u_{CE} voltage can be expressed due to u_1–u_3 voltages on the capacitances C_1–C_3 as follows:

$$u_{\text{CE}} = u_1 + u_2 = R_3 i_3 + u_3, \quad (7)$$

then, taking into account in (2)–(4) expressions (5), (6), the formulas can be obtained for the calculation of the capacitances values as functions of voltages on the latter and the current i_3:

$$C_1(u_1, u_2) = C_{\text{resh}} + C_{\text{res0}}(1 + u_1 + u_2)^{-k_{\text{res}}}; \quad (8)$$

$$C_2(u_1,u_2)=C_{ies}-C_{resh}-C_{res0}(1+u_1+u_2)^{-k_{res}}; \quad (9)$$

$$C_3(u_3,i_3)=C_{\text{oesh}}-C_{\text{resh}}+C_{\text{oes0}}(1+R_3i_3+u_3)^{-k_{\text{oes}}}- -C_{\text{res0}}(1+R_3i_3+u_3)^{-k_{\text{res}}}. \quad (10)$$

The current i_1 through the capacitance C_1 can be calculated in accordance with the following expression:

$$i_1=d[C_1(u_1,u_2)\cdot u_1]/dt, \quad (11)$$

considering the expression (8) for C_1, after transformations the dependence of current i_1 on the voltage drops u_1, u_2 can be obtained:

$$i_1=C_{\text{d1}}(u_1,u_2)\cdot du_1/dt, \quad (12)$$

where $C_{d1}(u_1, u_2)$ – the dynamic capacitance between the collector and the gate of the transistor, which is:

$$C_{d1}(u_1,u_2)=F_1(u_1,u_2)\cdot u_1+C_1(u_1,u_2), \quad (13)$$

in which $F_1(u_1, u_2)$ is a partial derivative of the capacitance $C_1(u_1, u_2)$ with respect to the voltage u_1, for which, according to (8), the following analytic expression can be obtained:

$$F_1(u_1,u_2)=\partial C_1(u_1,u_2)/\partial u_1= =-k_{\text{res}}C_{\text{res0}}(1+u_1+u_2)^{-k_{\text{res}}-1}. \quad (14)$$

The currents i_2, i_3 by analogy with (11) are possible to introduce by the following expressions:

$$i_2=C_{\text{d2}}(u_1,u_2)\cdot du_2/dt; \quad (15)$$

$$i_3=C_{\text{d3}}(u_3,i_3)\cdot du_3/dt, \quad (16)$$

where $C_{d2}(u_1, u_2)$, $C_{d3}(u_1, u_2)$ – the transistor dynamic capacitances between the gate and the emitter, the collector and the emitter, respectively, which are:

$$C_{\text{d2}}(u_1,u_2)=F_2(u_1,u_2)\cdot u_2+C_2(u_1,u_2); \quad (17)$$

$$C_{\text{d3}}(u_3,i_3)=F_3(u_3,i_3)\cdot u_3+C_3(u_3,i_3), \quad (18)$$

in which connection:

$$F_2(u_1,u_2)=\partial C_2(u_1,u_2)/\partial u_2= =k_{res}C_{res0}(1+u_1+u_2)^{-k_{res}-1}; \quad (19)$$

$$F_3(u_3,i_3)=\partial C_3(u_3,i_3)/\partial u_3= =-k_{oes}C_{oes0}(1+R_3i_3+u_3)^{-k_{oes}-1}+ +k_{res}C_{res0}(1+R_3i_3+u_3)^{-k_{res}-1}. \quad (20)$$

For a mathematical description of the reverse diode, the Ma-Lauritzen model can be used, which takes into account the process of reverse recovery:

$$\begin{cases} i_D=(q_E-q_M)/T_M; \\ q_E=I_s\cdot\tau\cdot[e^{u_D/(nU_T)}-1]; \\ dq_M/dt=i_D-q_M/\tau, \end{cases} \quad (21)$$

where i_D, u_D – the current through the diode and the voltage drop on the diode, respectively; q_E – the injected charge level at the junction; q_M – the total stored charge; T_M – approximate diffusion transit time; I_s – diffusion leakage current; τ – carrier lifetime; n – emission coefficient; U_T – the temperature potential of the p-n junction.

According to the system of equations (21), the diode can be represented by a controlled current source $i_D(u_D)$.

5. Mathematical model of single-phase half-bridge inverter with resistive load

Let us look at the construction of a mathematical model for an elementary semiconductor converter with IGBT – a single-phase half-bridge inverter (Fig. 2). Such converter is an integral part of a widespread three-phase autonomous voltage inverter, known to be used in a frequency controlled electric drive, therefore the proposed simulation technique can be used during research into processes in a three-phase system. The circuit diagram of the inverter includes two ideal sources of EMF u_1, u_2, to which VT1 and VT2 transistors are connected in series, with the reverse diode VD1, VD2, respectively. The resistive load R_0 is connected between the middle point of the power supply and the node, in which VT1 emitter and VT2 collector are connected. The gates of the transistors VT1 and VT2 are fed by pulse EMF from the controlled voltage sources u_{G1} and u_{G2} through the ballast resistors R_{G1} and R_{G2}, respectively, which represent drivers.

Taking into account in the circuit diagram of the inverter (Fig. 2), the IGBT (Fig. 1) and diode equivalent circuits, the equivalent circuit of single-phase half-bridge inverter can be obtained (Fig. 3), for the analysis of which the graph-analytical method can be used. The following equivalent circuit consists of 11 nodes connected by 19 single-component branches (voltage and current sources, resistances and capacitances), a "node" means a connection of two or more branches. For a graph of the equivalent circuit, using the algorithm described in [11], a tree that includes 11 edges (relevant branches b_1–b_{11} are marked with thick lines in Fig. 3) and the complement of the tree (includes 10 chords: b_{12}–b_{21}) are constructed. The tree includes independent voltage sources U_{G1}, U_1, U_{G2}, U_2, capacitive branches C_{11}, C_{21}, C_{31}, C_{12}, C_{22}, C_{32} and resistive branch R_{U2}. The complement of the tree is formed by resistive branches R_{G1}, R_{31}, R_0, R_{G2}, R_{32}, R_{u1} and controlled current sources I_{c1}, i_{D1}, I_{c2}, i_{D2}.

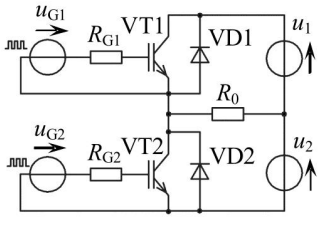

Fig. 2. Circuit diagram of the single-phase half-bridge inverter with resistive load

The matrix of the main sections **F**, that is calculated on the basis of the first incidence matrix and establishes the connection between the edges and the main sections of the graph, defines a complete system of topological equations that describes the electric circuit in accordance with the Kirchhoff's laws. For the graph of the underlying equivalent circuit, the matrix of the main sections includes the sub-matrices $\mathbf{F}_1$,..., $\mathbf{F}_6$, which de-

scribe the connection between the corresponding edges and chords:

$$\mathbf{F} = \begin{array}{c|cc} & \{R_{ch}\} & \{I_{cnt}\} \\ \hline \{U\} & \mathbf{F}_1 & \mathbf{F}_4 \\ \{C_{ed}\} & \mathbf{F}_2 & \mathbf{F}_5 \\ \{R_{ed}\} & \mathbf{F}_3 & \mathbf{F}_6 \end{array}, \quad (22)$$

where $\{U\}$, $\{I_{cnt}\}$ – the sets of independent voltage sources and controlled current sources; $\{R_{ed}\}$, $\{R_{ch}\}$ – the sets of resistive edges and chords; $\{C_{ed}\}$ – the set of capacitive edges; submatrix $\mathbf{F}_4$ is zero since current sources and voltage sources are mutually unrelated.

The numerical value of the matrix of the main sections for the graph of the equivalent circuit of the inverter (Fig. 3), obtained as a result of using the known algorithm for calculating **F** [11], is given in Table 1.

The equations of vectors of resistive edges currents $\mathbf{I}_{Red}$ and resistive chords voltages $\mathbf{U}_{Rch}$, compiled according to the matrix of the main sections (22), are:

$$\mathbf{I}_{\mathrm{R}ed} = -\mathbf{F}_3 \cdot \mathbf{I}_{Rch} - \mathbf{F}_6 \cdot \mathbf{I}_{cnt}; \quad (23)$$

$$\mathbf{U}_{Rch} = \mathbf{F}_1^{\mathrm{T}} \cdot \mathbf{U} + \mathbf{F}_2^{\mathrm{T}} \cdot \mathbf{U}_{Ced} + \mathbf{F}_3^{\mathrm{T}} \cdot \mathbf{U}_{\mathrm{R}ed}, \quad (24)$$

where $\mathbf{U}=[u_{G1}\ u_1\ u_{G2}\ u_2]^{\mathrm{T}}$ – vector of independent voltage sources; $\mathbf{I}_{cnt}=[I_{c1}\ i_{D1}\ I_{c2}\ i_{D2}]^{\mathrm{T}}$ – vector of controlled current sources; $\mathbf{U}_{Ced}=[u_{11}\ u_{21}\ u_{31}\ u_{12}\ u_{22}\ u_{32}]^{\mathrm{T}}$ – vector of capacitive edges voltages; $\mathbf{I}_{\mathrm{R}ch}=[i_{RG1}\ i_{R31}\ i_0\ i_{RG2}\ i_{R32}\ i_{\mathrm{R}u1}]^{\mathrm{T}}$, $\mathbf{U}_{Rch}=[u_{RG1}\ u_{R31}\ u_0\ u_{RG2}\ u_{R32}\ u_{\mathrm{R}u1}]^{\mathrm{T}}$ – vectors of resistive chords currents and voltages, respectively; $\mathbf{I}_{Red}=[i_{Ru2}]$, $\mathbf{U}_{Red}=[u_{Ru2}]$ – vectors of resistive edges currents and voltages, respectively, which, in this case, include one element, since only one resistive branch R_{U2} is assigned to the graph tree; the "T" symbol denotes transposition.

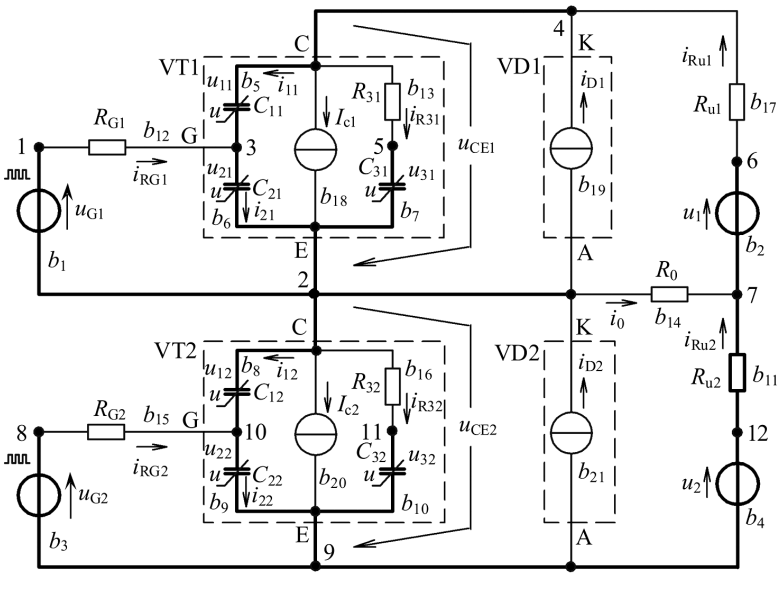

Fig. 3. Equivalent circuit of the single-phase half-bridge inverter with resistive load, which indicates the nodes (1–12) and the branches b_1–b_{21} of the graph (b_1–b_{11} – the edges marked with thick lines, b_{12}–b_{21} – chords)

According to the Ohm's law, the vectors of resistive edges voltages $\mathbf{U}_{Red}$ and resistive chords currents $\mathbf{I}_{\mathrm{R}ch}$ are calculated by using the diagonal matrixes of resistive edges $\mathbf{R}_{ed}$ and chords $\mathbf{R}_{ch}$:

$$\mathbf{U}_{\mathrm{R}ed} = \mathbf{R}_{ed} \cdot \mathbf{I}_{\mathrm{R}ed}, \quad (25)$$

$$\mathbf{I}_{Rch} = \mathbf{R}_{ch}^{-1} \cdot \mathbf{U}_{Rch}, \quad (26)$$

and $\mathbf{R}_{ch}=\mathrm{diag}\{R_{G1}\ R_{31}\ R_0\ R_{G2}\ R_{32}\ R_{u1}\}$, $\mathbf{R}_{ed}=\mathrm{diag}\{\mathrm{R}_{u2}\}$.

The vector $\mathbf{I}_{Ced}=[i_{11}\ i_{21}\ i_{31}\ i_{12}\ i_{22}\ i_{32}]^{\mathrm{T}}$ of capacitive edges currents is determined by the matrix of the main sections in the following way:

$$\mathbf{I}_{Ced} = -\mathbf{F}_2 \cdot \mathbf{I}_{Rch} - \mathbf{F}_5 \cdot \mathbf{I}_{cnt}. \quad (27)$$

Table 1

The matrix of the main sections for the graph of the equivalent circuit (Fig. 3)

F		chords									
		R_{G1}	R_{31}	R_0	R_{G2}	R_{32}	R_{u1}	I_{c1}	i_{D1}	I_{c2}	i_{D2}
edges	u_{G1}	1	0	0	0	0	0	0	0	0	0
	u_1	0	0	0	0	0	1	0	0	0	0
	u_{G2}	0	0	0	1	0	0	0	0	0	0
	u_2	0	0	−1	0	0	1	0	0	0	0
	C_{11}	0	1	0	0	0	−1	1	−1	0	0
	C_{21}	−1	1	0	0	0	−1	1	−1	0	0
	C_{31}	0	−1	0	0	0	0	0	0	0	0
	C_{12}	0	0	1	0	1	−1	0	0	1	−1
	C_{22}	0	0	1	−1	1	−1	0	0	1	−1
	C_{32}	0	0	0	0	−1	0	0	0	0	0
	R_{u2}	0	0	1	0	0	−1	0	0	0	0

The voltages on capacitive branches are state variables of the inverter. The equation of state of reactive elements has the form:

$$\mathbf{I}_{Ced} = \mathbf{\Phi}(\mathbf{U}_{Ced}, \mathbf{I}_{Rch}) \cdot d\mathbf{U}_{Ced} / dt, \quad (28)$$

where $\mathbf{\Phi}(\mathbf{U}_{Ced}, \mathbf{I}_{Rch})$ – the diagonal matrix of IGBT dynamic capacitances.

The values of the matrix $\mathbf{\Phi}$ elements depend on the voltages on the capacitances and currents of the resistive chords according to the dependences (13), (17), (18), namely:

$$\mathbf{\Phi}(\mathbf{U}_{\mathrm{C}ed}, \mathbf{I}_{\mathrm{R}ch}) = \mathrm{diag}\{C_{\mathrm{d}11}\ \ C_{\mathrm{d}21}\ \ C_{\mathrm{d}31}\ \ C_{\mathrm{d}12}\ \ C_{\mathrm{d}22}\ \ C_{\mathrm{d}32}\}. \quad (29)$$

The matrix differential equation of state of the inverter relative to the vector $\mathbf{U}_{\mathrm{C}ed}$ of state variables in accordance with (28) is:

$$d\mathbf{U}_{Ced} / dt = \mathbf{\Phi}^{-1}(\mathbf{U}_{Ced}, \mathbf{I}_{Rch}) \cdot \mathbf{I}_{Ced}, \quad (30)$$

where $\mathbf{\Phi}^{-1}(\mathbf{U}_{\mathrm{C}ed}, \mathbf{I}_{\mathrm{R}ch})$ – inverse matrix of IGBT dynamic capacitances, which is:

$$\mathbf{\Phi}^{-1}(\mathbf{U}_{\mathrm{C}ed}, \mathbf{I}_{\mathrm{R}ch}) = \mathrm{diag}\{C_{\mathrm{d}11}^{-1}\ \ C_{\mathrm{d}21}^{-1}\ \ C_{\mathrm{d}31}^{-1}\ \ C_{\mathrm{d}12}^{-1}\ \ C_{\mathrm{d}22}^{-1}\ \ C_{\mathrm{d}32}^{-1}\}. \quad (31)$$

During the numerical solution of equation (30), it is necessary to calculate the value of the vector $\boldsymbol{I}_{cnt}$ of controlled current sources at each step of integration, which is used in the equations (23) and (27). The calculation of source

currents I_{c1} and I_{c2}, corresponding to the nonlinear static volt-ampere characteristics of IGBT, is carried out according to (1). This, according to (7), determines the functional dependence of the $\mathbf{I}_{cnt}$ vector on $\mathbf{U}_{Ced}$. The calculation of diode currents i_{D1}, i_{D2} is carried out in accordance with the first equation of the system (21). Since these currents are determined by the values of total charges q_{M1}, q_{M2}, then, combining the latter with the vector $\mathbf{Q}_M=[q_{M1}\ q_{M2}]^{\mathrm{T}}$, it is true to say that the $\mathbf{I}_{cnt}$ vector depends also on $\mathbf{Q}_M$:

$$\mathbf{I}_{cnt}=\mathbf{I}_{cnt}(\mathbf{U}_{Ced},\mathbf{Q}_M). \quad (32)$$

In this case, the $\mathbf{Q}_M$ vector can be calculated by the matrix differential equation, which is based on the third equation of the system (21):

$$d\mathbf{Q}_M/dt=\mathbf{T}_1\cdot\mathbf{Q}_M+\mathbf{T}_2\cdot\mathbf{Q}_E, \quad (33)$$

where

$$\mathbf{T}_1=\mathrm{diag}\{-T_{M1}^{-1}-\tau_1^{-1}\quad T_{M2}^{-1}-\tau_2^{-1}\};$$

$$\mathbf{T}_2=\mathrm{diag}\{T_{M1}^{-1}\quad T_{M2}^{-1}\};$$

$$\mathbf{Q}_E=[q_{E1}\quad q_{E2}]^{\mathrm{T}}.$$

Each element q_{Ej} (j=1, 2) of the $\mathbf{Q}_E$ vector, according to the second equation of the system (21), depends on the voltages u_{Dj} applied to the j-th diode. According to the equivalent circuit (Fig. 3) of the converter, $u_{Dj}=-u_{1j}-u_{2j}$, which determines the dependence of $\mathbf{Q}_E$ on $\mathbf{U}_{Ced}$:

$$\mathbf{Q}_E=\mathbf{Q}_E(\mathbf{U}_{Ced}). \quad (34)$$

The model output values are: currents i_{RG1}, i_{RG2} of gates; currents $i_{k1}=i_{11}+I_{c1}+i_{31}$ and $i_{k2}=i_{12}+I_{c2}+i_{32}$ of the collectors of transistors VT1 and VT2, respectively; load current i_0. These values can be combined into a vector of desired currents:

$$\mathbf{Y}_1=[i_{RG1}\quad i_{RG2}\quad i_{k1}\quad i_{k2}\quad i_0]^{\mathrm{T}}. \quad (35)$$

It is also necessary to determine the voltages u_{21}, u_{22}, u_{CE1}, u_{CE2}, and the voltage u_0 on the load, which can be combined into the vector of the desired voltages:

$$\mathbf{Y}_2=[u_{21}\quad u_{22}\quad u_{CE1}\quad u_{CE2}\quad u_0]^{\mathrm{T}}. \quad (36)$$

The values of the vectors of desired variables can be calculated as follows:

$$\mathbf{Y}_1=\mathbf{A}_1\cdot\mathbf{X}_1; \quad (37)$$

$$\mathbf{Y}_2=\mathbf{A}_2\cdot\mathbf{X}_2, \quad (38)$$

where $\mathbf{A}_1$, $\mathbf{A}_2$ – matrix constants; $\mathbf{X}_1$, $\mathbf{X}_2$ – vectors of currents and voltages, respectively, of the equivalent circuit branches of a single-phase half-bridge inverter in accordance with Fig. 3, which are equal:

$$\mathbf{X}_1=[\mathbf{I}_{Red}\quad \mathbf{I}_{Rch}\quad \mathbf{I}_{Ced}\quad \mathbf{I}_{cnt}]^{\mathrm{T}}, \quad (39)$$

$$\mathbf{X}_2=[\mathbf{U}_{Red}\quad \mathbf{U}_{Rch}\quad \mathbf{U}_{Ced}]^{\mathrm{T}}. \quad (40)$$

Thus, the equivalent circuit of a single-phase, half-bridge inverter with resistive load (Fig. 3) is described by a system of matrix differential equations of state (30), (33), equations (23)–(27), (31), (32), (34) and the output equations (37), (38).

6. Simulink model of semiconductor converter

Let us consider the block diagram of the Simulink model of the single-phase half-bridge inverter with pulse-width modulation of output voltage, that implements the mathematical model (Fig. 4). Subsystem 1 is intended for generation of a discrete signal f, which specifies the state of the inverter transistors VT1, VT2. The subsystem includes generator $G1$ of the sawtooth reference voltage u_{ref} with carrier frequency f_{ref} (which provides one-side modulation of the output voltage of the converter) and a sinusoidal voltage generator u_{st} of the setpoint voltage (frequency f_{st}). These voltages are fed to the null device $Z1$, whose output signal f=1 corresponds to the VT1 open state and the VT2 closed state, and f=−1 – the inverse combination of states of the switches.

The blocks 2 and 3 form the control signals of the power switches, which include the relay elements F1 and F2, respectively, with mutually inverse characteristics. These elements divide the signal f by two channels and generate the signals f_1 and f_2, the low level of each of which corresponds to the closed state of the switch, high level – to the open state. Also, formers 2 and 3 include DT1 and DT2 blocks of switch delays. These blocks provide a delay of the rising edge of the output signals f_{d1} and f_{d2} relative to f_1 and f_2, respectively, to prevent short circuits during switching of the IGBTs.

Blocks D1 and D2 simulate drivers, which, according to the logic signals f_{d1} and f_{d2}, generate the control voltages u_{G1} and u_{G2} of the transistors VT1 and VT2. These voltages, together with the voltage u_1, u_2 of power sources, are combined by unit 4 into the vector of independent power supplies $\mathbf{U}$. Subsystem 5 is designed for calculating the values of $\mathbf{U}_{\mathrm{Rch}}$ vector of resistive chords voltages according to (24). In block 6, the values of the $\mathbf{I}_{\mathrm{Rch}}$ vector of the resistive chords currents are calculated in accordance with (26). Subsystem 7 is used to calculate the values of vector $\mathbf{I}_{\mathrm{Red}}$ of resistive edge currents in accordance with (23). Block 8 is used to calculate the values of the vector $\mathbf{U}_{\mathrm{Red}}$ of the resistive edge voltages as (25).

Subsystem 9 is designed for calculating the matrix $\mathbf{\Phi}^{-1}(\mathbf{U}_{\mathrm{Ced}},\mathbf{I}_{\mathrm{Rch}})$ values in accordance with (31) using (13), (17), (18). In subsystem 10, the values of the $\mathbf{I}_{Ced}$ vector of capacitive ribs currents are calculated according to (27). The values of the $\mathbf{I}_{cnt}$ vector on the basis of (32) and the values of the $\mathbf{Q}_{\mathrm{E}}$ vector according to the dependence (34) are calculated in subsystem 11.

Subsystems 12 and 13, which integrate the right-hand parts of the matrix differential equations (30) and (33), are used to calculate the $\mathbf{U}_{Ced}$ and $\mathbf{Q}_M$ vectors of state variables, respectively, under initial conditions $\mathbf{U}_{Ced}(0)$ and $\mathbf{Q}_M(0)$. The calculation of the values of the vectors $\mathbf{Y}_1$ and $\mathbf{Y}_2$ of the required variables is carried out according to the equations (37) and (38), the corresponding subsystems in Fig. 4 are not shown.

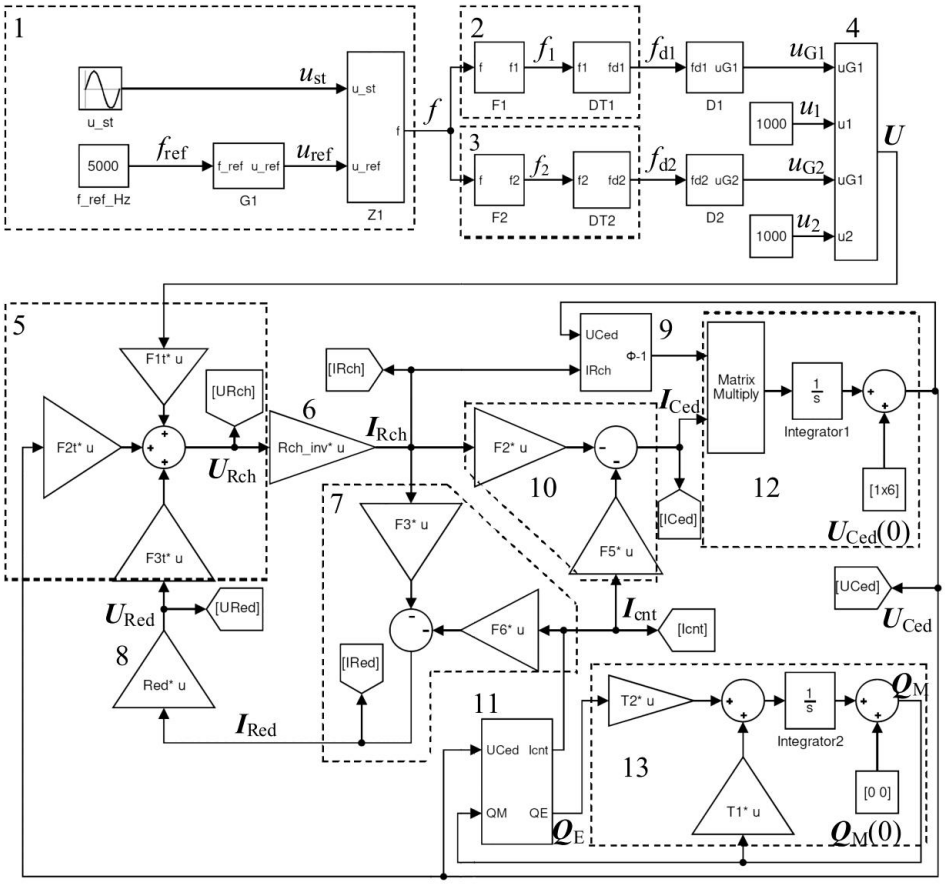

Fig. 4. The block diagram of the single-phase half-bridge inverter model

IGBT transistors with built-in diodes 5SNA2000K450300 of ABB [12] are considered for numerical simulation. The parameter values, discovered in accordance with the datasheet, are as follows. For the diode: T_M=1.06 μs; τ=1.83 μs; I_s=1·10^{-9} s; nU_T=0.54 V. For the transistor: u_{Th}=7 V; u_D=1 V; k=250 V; R_3=1 Ω; C_{resh}=3.1 nF; C_{res0}=160 nF; k_{res}=1.56; C_{oesh}=8 nF; C_{oes0}=240 nF; k_{oes}=1,57; C_{ies}=220 nF. The simulation was carried out at the source voltage u_1=u_2=1000 V and their internal resistance R_{u1}=R_{u2}=0,01 Ω, load value R_0=100 Ω. The transistors were controlled by the voltages of the sources u_{G1} and u_{G2}, and the voltage −2 V corresponds to the transistor closed state, 15 V – open state. Ballast resistors R_{G1}=R_{G2}=1,5 Ω. The frequency of the setpoint voltage is taken f_{st}=50 Hz, the frequency of the reference voltage of the pulse-width modulation f_{ref}=5 kHz. Calculations were carried out by the backward differentiation method (solver ode23tb), and the integration step did not exceed 5·10^{-10} s. The switching processes of the IGBT were simulated during one setpoint voltage period, which corresponds to 20 ms.

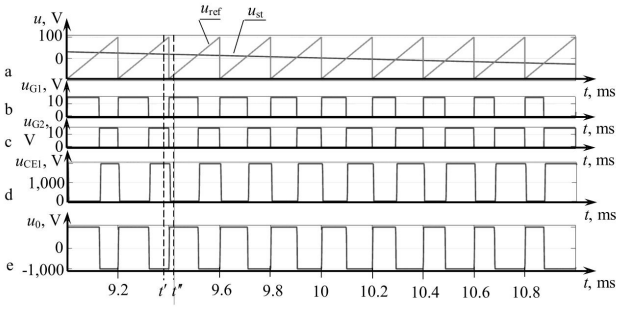

Fig. 5. The graphs obtained by simulating the operation of a single-phase half-bridge inverter with resistive load in case of one-sided pulse-width modulation of the output voltage as a function of time t: a – reference voltage u_{ref} and setpoint voltage u_{st}; b, c – control voltages u_{G1} and u_{G2}, which are formed by drivers of transistors VT1 and VT2, respectively; d – voltage u_{CE1} of VT1; e – voltage u_0 on load R_0; transients during the interval from t'=9.399 ms to t''=9.404 ms are illustrated in Fig. 6

7. Discussion of the results of an analysis of power switches commutation of a single-phase half-bridge inverter

The graphs, shown in Fig. 5, 6, were obtained as a result of the simulation. The graphs illustrate the function of the proposed model of a single-phase half-bridge inverter with resistive load in the mode of pulse-width modulation of the output voltage.

The generator G1 forms a reference voltage u_{ref}, which has an antisymmetric sawtooth character at each modulation period $1/f_{ref}$=0.2 ms. This, when changing the setpoint voltage u_{st}, provides the offset of the falling edge of transistor VT1 control voltage u_{G1}, rising edge of the transistor VT2 control voltage u_{G2} and falling edge of load voltage u_0. When one of the switches is in the closed state, the voltage between collector and emitter of another reaches the level u_1+u_2=2,000 V.

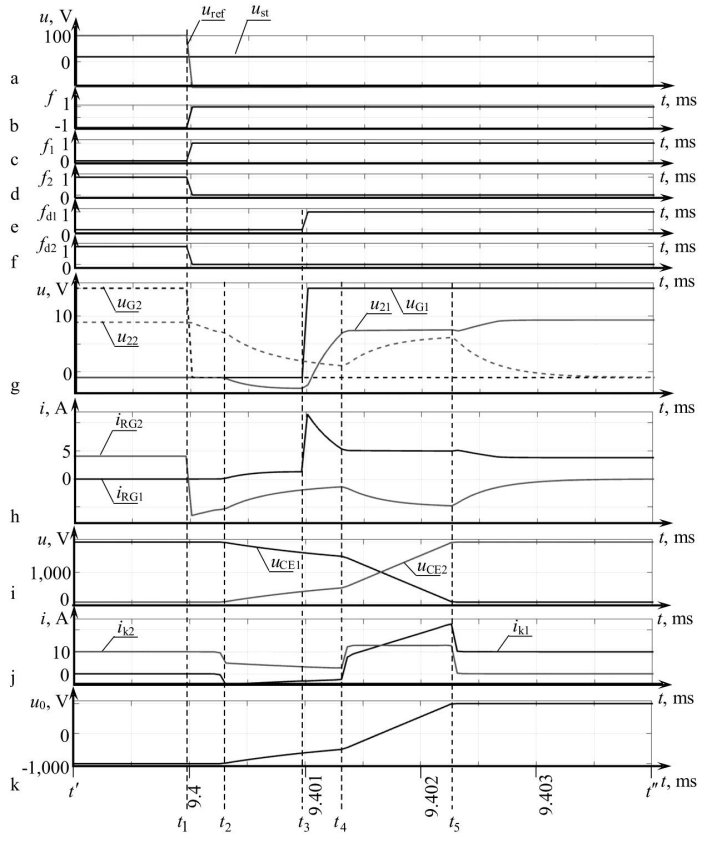

Fig. 6. The graphs of transients during IGBT switching of a single-phase half-bridge inverter on time *t*: a — reference u_{ref} and setpoint u_{st} voltages; b — signal *f*; c, d — control signals f_1 and f_2; e, f — control signals f_{d1} and f_{d2} of the power switches; g — control voltages u_{G1} and u_{G2} and the voltage u_{21} and u_{22} of the transistors gates; h — currents i_{RG1} and i_{RG2} of gates; i — voltages u_{CE1} and u_{CE2}; j — currents i_{k1} and i_{k2} of collectors of VT1 and VT2, respectively; k — voltage u_0 on the load R_0

The graphs in Fig. 6 allow to analyze the transients of transistor VT2 closing and the subsequent VT1 opening in more detail, as reflecting the time interval from t'=9.399 ms to t''=9.404 ms.

At the beginning of this interval, the reference voltage u_{ref} exceeded the setpoint voltage u_{st}, which determined the closed state of the transistor VT1 and the open state of VT2, the voltage at the load u_0=−1,000 V. At t_1 moment u_{ref} becomes less than u_{st}, which is detected by the null device Z1, which output signal *f* changes from −1 to 1, the signals f_1 and f_2 at the outputs of the relay elements F1 and F2 change, respectively, giving commands for closing VT2 and opening VT1. The falling edge of the VT2 closing signal passes through the block DT2 without delay – the signal f_{d2} duplicates f_2, decreasing to 0 at the t_1 moment. However, the rising edge of the VT1 opening signal is delayed by the unit DT1 for t_3−t_1=1 μs (f_{d1} varies at time t_3). This prevents short circuits between power bars.

The control voltage u_{G2} decreases with the driver circuit at the time t_1 from 15 V to −2 V, which initiates the closing transient process of VT2. From the t_1 moment, the capacitance C_{21} between the gate and the emitter of VT2 starts to discharge, the voltage u_{22} at which exponentially decreases, reaching the threshold value u_{Th}=7 V at time t_2. The i_{RG2} current, flowing through the gate, at the time t_1 changes the sign, jumping down to i_{RG2}=−7 A, and, as the capacitance C_{21} is discharging, its absolute value decreases. Since, until t_2, the gate voltage u_{22} was greater than the threshold value u_{Th}=7 V, the voltage u_{CE2} between the collector and emitter of the transistor remained at a constant level. In this case, the current i_{k2} of the VT2 collector also does not change, remaining on 10 A level.

After t_2 moment, the closing process of the VT2 transistor starts, which is accompanied by a discharge of capacitances C_{12} and C_{32}. The voltage u_{22} and the absolute value of collector current i_{k2} continue to exponentially decrease, the voltage u_{CE2} begins to increase, the current i_{k2} of the VT2 collector decreases. Accordingly, the u_{CE1} voltage, which at the time t_2 was 2,000 V, after the start of VT2 closing begins to decrease. The decrease of u_{21} voltage at the VT1 gate, current i_{k1} and a slight increase in the i_{RG1} current after t_2 are due to the processes of capacitances C_{12} and C_{32} discharge and the redistribution of voltages on the transistors. The voltage at the load, which by the time t_2 was u_0= 1,000 V, began to increase after VT2 closing process starts. At time t_3, the signal f_{d1} is sent to open VT1, and the voltage u_{G1} at the driver D1 output increases from 2 V to 15 V, the C_{21} charge process begins, the voltage u_{21} exponentially increases. The i_{RG1} current of the VT1 gate at time t_3 is stepwise changed to 12 A, and then exponentially decreases with C_{21} charge. By the time t_4, VT1 remains closed, at the given moment u_{21} reaches the threshold u_{Th} and the process of reducing the resistance of the VT1 starts. On the [t_4, t_5] interval, while the voltage u_{CE1} decreases to 0, the charge of spurious capacitance C_{11} (Miller capacitance) between the VT1 collector and gate occurs. In this case, the u_{21} voltage remains at a constant level, which is called the Miller plateau. This is accompanied by the current i_{k1} increasing to 22 A at the time t_5, which is more than 2 times the operating level of the open transistor current in this circuit (10 A) and, under certain conditions, can reduce the resource of the semiconductor device. After t_5 moment, the load voltage u_0 reaches the level of 1,000 V, and the processes of recharging spurious capacitances of transistors continue for about 1 μs. Thus, under given conditions, the process of switching the IGBTs of a single-phase inverter lasts about 4 μs.

The reliability of the obtained results is provided by the validity of the accepted assumptions, the use of proven methods of theoretical research and the satisfactory coincidence of the results of theoretical studies with the experimental data obtained in [10]. The deviation of the parameters did not exceed 5–7 %.

The given results are obtained in the operation of a single-phase inverter with resistive load, provided that there is no higher harmonics in the input voltage. During the further research, it is expedient, using the proposed methodology, to form a mathematical model of a three-phase IGBT inverter, which feeds an asynchronous motor. This will enable to investigate the harmonic composition of the leakage current to the ground in the variable frequency circuit and to assess the electrical safety of the power supply system.

8. Conclusions

1. The mathematical model of the insulated-gate bipolar transistor in the IGBT module was improved due

to the determination of analytical expressions for dynamic capacitances between the leads of the device. This simplifies the accounting for the overcharging of these capacitances during a dead time when commutation of adjacent switches in the model. Such approach allows us to investigate high-frequency transient components of currents and voltages in electrical systems with semiconductor converters.

2. The method of forming a mathematical model of the IGBT voltage inverter in the form of matrix differential equations of state in the Cauchy form and nonlinear equations is proposed. The application of this method is illustrated by the example of a single-phase half-bridge inverter with resistive load. The obtained mathematical model differs from the well-known in advanced representation of separate elements by nonlinear differential equations and taking into account mutual influences.

3. The peculiarities of the IGBT inverter switching transients are revealed, in particular, the significant exceeding (more than twice) of the transistor current during opening the operating current at the end of the switching process, which can reduce the resource of the device.

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