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Запропоновано спосіб підвищення завадостійкості детектора фазоманіпульованих (ФМ) сигналів на основі пристрою фазового автопідстроювання частоти (ФАПЧ) шляхом використання його модифікації.

Задача підвищення завадостійкості систем зв'язку до цих пір йшла в протиріччі із завданням досягнення високих динамічних показників пристрою для ефективної та коректної обробки ФМ-сигналів з великим індексом модуляції. Покращення завадостійкості системи означало погіршення її динамічної поведінки і навпаки. Запропонований спосіб дає можливість знизити шумовий поріг пристрою, не погіршуючи при цьому його динамічних властивостей.

Імітаційне моделювання граничної завадостійкості класичного та модифікованого пристроїв проводилось для двох критеріїв зриву синхронізації. В обох випадках завадостійкість модифікованого пристрою є кращою. Результати імітаційного моделювання показують, що аномальні стрибки фази опорного генератора модифікованого пристрою за короткий час спостерігаються для більших рівнів шуму, ніж в класичному пристрої (на 1,5–4 дБ залежно від параметрів пристрою).

Обидва варіанти пристроїв були фізично реалізовані на базі програмованої логічної інтегральної схеми (ПЛІС) з метою проведення експериментальних досліджень завадостійкості цих пристроїв та перевірки результатів імітаційного моделювання. Експериментальні дослідження якісно підтвердили результати моделювання та показують, що використання модифікованого фазового детектора дає виграш у завадостійкості на 1–2,5 дБ залежно від параметрів пристрою. Динамічні властивості модифікованого пристрою при цьому не погіршуються.

Наведені результати демонструють неабиякі перспективи використання пристроїв ФАПЧ з підвищеною завадостійкістю у системах зв'язку різноманітного призначення, що працюють в складній завадовій обстановці

Ключові слова: пристрій фазового автопідстроювання частоти (ФАПЧ), модифікований фазовий детектор (ФД), вузькосмуговий фільтр (ВСФ)

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FIRMWARE IMPLEMENTATION AND EXPERIMENTAL RESEARCH OF THE PHASE-LOCKED LOOP WITH IMPROVED NOISE IMMUNITY

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1. Introduction

Today, it is impossible to imagine a modern society without such innovations as the Internet, digital TV, mobile phones, GPS, etc. The emergence and development of these technologies would be impossible without progress in the field of radio engineering, microelectronics and digital circuitry. However, despite their complexity, these devices

have become the everyday elements of our lives. The radio equipment is becoming more functional, more reliable and at the same time more compact. New algorithms for signal processing and new modulation methods enable communication systems to use the frequency range more efficiently, which gives an opportunity to increase the number of users and reduce the cost of system operation.

Nevertheless, there is a certain limit that narrows further development of radio electronic devices and systems. The limit is determined by the threshold value of the signal-to-noise ratio (SNR), the passing of which causes the system to lose efficiency. This threshold determines the capacity of the system, meaning, the maximum number of users, for which the system can still provide the minimum required quality of operation (communication). This relationship is described by the Viterbi formula [1], according to which it is necessary to reduce the SNR threshold value, for which the system still maintains efficiency, to increase the capacity of the system.

Thus, one of the ways to increase the system capacity without extending the frequency range of its operation is to increase its noise immunity. Due to the fact that the most modern radioelectronic systems (radar, radio navigation, and telecommunications) operate in a complex noisy environment, scientific studies related to the noise immunity improvement of such systems are today an actual scientific objective. A key element of these systems, which determine performance and reliability under such conditions, is the phase-locked loop (PLL). Therefore, improvement of its critical noise immunity will allow reaching a new level of operation quality of radio electronic devices and communication systems in various spheres (both military and civilian).

Due to the widespread application of modern communication systems (especially new generation 3G and 4G wireless systems), the ever-increasing number of users of such systems and the increasing amount of data (which doubles almost every year) transmitted by these systems, it is important to ensure their high-quality independent operation [2]. Under conditions of the limited frequency range, this problem can be solved by improving the noise immunity of each device in the network. Therefore, the research topic of the PLL noise immunity improvement (in terms of providing efficiency for significantly lower SNR than in known devices) with simultaneous maintenance of the power consumption and used frequency ranges is important and relevant.

2. Literature review and problem statement

The analysis of noise and dynamic effects on analog PLL shows contradictory requirements for device parameters. In particular, in [3, 4], approximate expressions to define SNR at the device output via device parameters and SNR at the device input were obtained. Analytical models of the classical device show that the increase of the device bandwidth allows processing signals with a large modulation index, but makes the device vulnerable to external random and deterministic noise signals. At the same time, reducing the device bandwidth improves its noise immunity, but worsens its dynamic characteristics.

Such a contradiction was solved in work [5]. This work offers a method to increase the PLL noise immunity by using a modified phase detector with additional narrowband filtering of an information signal from noise. Simulation has shown that the noise threshold of a modified PLL is significantly reduced for signals with high modulation index, and nonlinear signal distortions at the output of the device are lower.

Indicated results proved their practical value in work [6], which shows the efficiency of the modified PLL application in systems with more complex types of phase manipulation. In addition, there are great perspectives to use a modified PLL with other modulation types, for example, amplitude modulation of many components (AMMC) [7]. AMMC is characterized by a higher potential noise immunity (in comparison with quadrature modulation) under the condition of the same input signal power [7].

The work [5] is similar to the work [8], which is devoted to the research of digital PLL statistical characteristics that takes into account the effects of noise and input signal modulation. The whole research in work [8] is carried out by simulation experiments. As well as in the previous case, the issue of noise immunity improvement was not considered in this work.

A separate case of working with pulse signals and noise immunity of reception of these signals is considered in the paper [9]. But it does not show the ways of applying the optimization results to digital PLLs.

With the development of digital electronics, the number of PLL types has significantly increased. In particular, [10] provides a detailed classification of digital PLLs and the work [11] gives the options of the PLL key component's implementation depending on their type. In modern worldwide technical literature, a lot of attention is devoted to the research of the PLL with non-uniform sampling techniques, which work with pulse signals, and their practical implementation for clock formation [12] or frequency synthesis with low phase noise [13]. The work [14] evaluates the phase noise of the signal at the device output under the influence of a noise signal at the device input for two types of such devices. Considering the complexity of mathematical models of this type of devices because of complex nonlinear processes during its operation, such class of devices is not considered in this article.

At the same time, these works do not consider the issue of external noise influence on the quality of synchronization. Even in the case of a classic analog PLL, the model of which is quite simple, the analysis of the simultaneous influence of random and deterministic noise is a complex mathematical problem that does not give exact mathematical solutions [8]. Therefore, the number of scientific works on this subject is very limited.

One of the works, which examines an improvement of the device synchronization quality in a complex noisy environment is work [5]. For this purpose, the author uses an additional module to estimate the current frequency of the input signal, which enables them to maintain synchronization at higher noise levels. However, this result is achieved by reducing the gain of the entire device loop and its bandwidth, which negatively affects its dynamic characteristics.

Despite the prospects of the obtained results and the practical value, the work[6] lacks experimental research, which shows the physical realization of real PLL devices. Therefore, there is a good reason to develop the achievements of previous studies for digital PLLs. There is also a need to implement such device by using modern software and hardware tools. The purpose of this implementation is to conduct experimental research of the supreme noise immunity of digital devices. In particular, the work [16] carries out the firmware implementation of the digital device and experimental study of the conditions for synchronization loss without noise influence. The authors have experimentally derived the criterion for the synchronization maintenance and also

demonstrated the effect of signal parasitic harmonics at the PD output on the PLL holding range, which is not described by the linearized model of the device. But the conditions for the synchronization breakdown under the influence of noise have not been investigated.

The current way of digital and all-digital PLLs implementation is the use of Direct Digital Synthesizers (DDS). The theory and practice of developing such devices are considered in works [17, 18], but without sufficient analysis of their noise immunity.

In the paper [19], the frequency response characteristics of the DDS-based PLL are analyzed, but it also does not consider the noise properties.

Thus, the above-mentioned works lack one of two aspects:

– methods of noise immunity improvement with simultaneous preservation of their dynamic properties have not been investigated [3, 4, 8, 10, 11, 16–19];

– there is no development of a real firmware digital PLL and experimental research (and not just simulation) of this device noise immunity [5–9, 14, 15].

Therefore, there are reasons to assume that the absence of any of these components in these works predetermines the necessity to carry out experimental research of methods of noise immunity improvement, which ensure the preservation of PLL dynamic behavior.

3. The aim and objectives of the study

The aim of this work is to develop an improved firmware implemented PLL with a reduced noise threshold (comparing to the classic device) and maintained dynamic properties. Application of this device in communication systems will increase the number of users of the system and also provides work in a noisier environment.

To achieve this aim, the following objectives were set:

– to develop firmware implementation of the improved PLL on the basis of the modified phase detector block diagram for further experimental research of its noise immunity;

– to set three sets of parameters of classical and modified devices and conduct simulation of both devices to compare their critical noise thresholds;

– to conduct an experimental research of noise immunity of classical and modified PLL for the same three sets of parameters to compare their critical noise thresholds;

– to investigate the dynamic properties of both devices by comparing the duration of transient processes at the DCO input in the moment of the information message change of the incoming QPSK signal.

4. Structure of classical and modified PLL and their firmware implementation

4. 1. Classical PLL

The classical PLL contains (Fig. 1): a phase detector (PD), a digital filter (DF), and a digitally-controlled oscillator (DCO), built on the basis of direct digital synthesis (DDS) technology [17, 18]. In the experimental device, these structural blocks are implemented by software and they operate with digital signals. In order to send analog signals to the device input and monitor the output signal on the oscilloscope in the circuit, there are analog-to-digital (ADC) and digital-to-analog (DAC) converters.

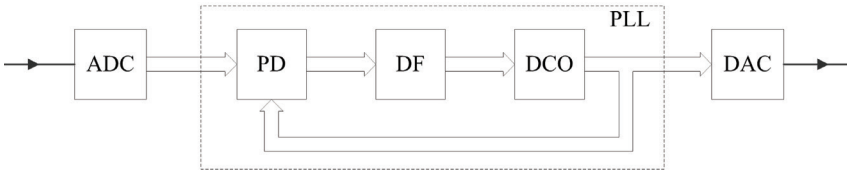


Fig. 1. Block diagram of the classical PLL [19]

The transfer function of the PLL closed loop is defined by the expression [11]:

$$H(s)=\frac{K_{PD}K_0H_{DF}(s)}{s+K_{PD}K_0H_{DF}(s)}, \quad (1)$$

where K_{PD}, K_0 are the transfer coefficients of PD and DCO, respectively, s is the complex variable, $H_{DF}(s)$ is the transfer function of DF.

This PLL contains a 1st order digital recursive filter, which is a prototype of the analog passive lead-lag filter with the transfer function:

$$H_A(s)=\frac{1+msT}{1+sT}, \quad (2)$$

where m is the proportionality coefficient, $T=1/2\pi f_c$ is the time constant, f_c is the cutoff frequency of the filter. The mechanism of calculation of DF coefficients is given in [19].

The transfer function of the device can also be expressed using normalized parameters ω_n and ζ – the natural frequency of the PLL and damping factor [11]. This pair of parameters gives a possibility to evaluate the shape of the PLL frequency response with high accuracy and estimate values in its key points [20]. The connection between the normalized parameters $\{\omega_n, \zeta\}$ and LPF parameters of the device is given in [19].

4. 2. Block diagram of the PLL with the modified phase detector

The modified PLL differs from the classical one by the presence of an additional block of the narrow-band filter (NBF, Fig. 2), which is located in front of the PD and designed to maximize filtering of the noise signal at the device input. Since the NBF suppresses also the section of the information signal spectrum, the modified PLL also contains a high-pass filter (HPF) located after the PD to compensate suppression of the information signal dynamic properties. When the random noise signal is present, the key reason for synchronization loss is that the noise peaks are beyond the range of the PD working area (±90°). The NBF is intended to reduce the peak values of noise nuisance to ensure that the PD works in its operating range.

The NBF block is a quadrature circuit, which transfers the frequency of the signal to the low-frequency range in order to filter the information signal from noise, and then transfers back the filtered signal to the carrier frequency range. Filtering is performed by using a digital 1st low-pass filter (LPF), the prototype of which is the analog passive lead-lag filter. Accordingly, the main parameters of the NBF are cutoff frequency and proportionality factor m_0.

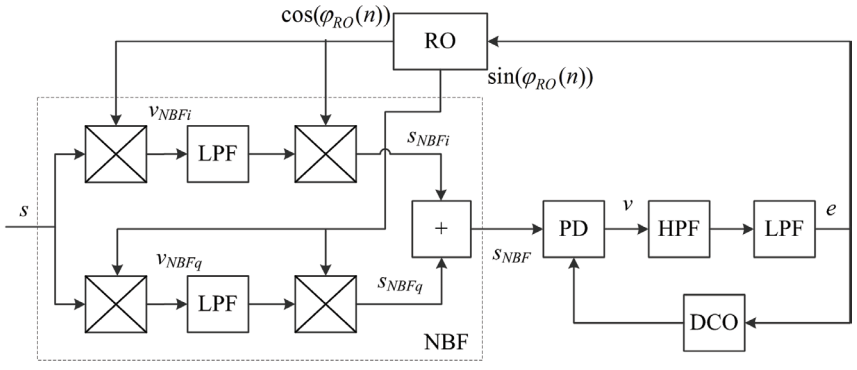


Fig. 2. Block diagram of the modified PLL with the modified phase detector

In order to restore the information signal spectrum correctly without distortions, it is necessary to select the right parameters of the HPF located after the detector. Its frequency response must be inverse to the NBF frequency response, i. e. $K_{NBF}(s)K_{HPF}(s)=\text{const}$. To ensure this condition, the HPF cut-off frequency should be selected using the expression $f_{HPF}=f_{NBF}/m_0$ (Fig. 3). The proportionality coefficients of both filters are equal. Thus, for any frequency, the product of both filters transfer functions is $K_{NBF}(s)K_{HPF}(s)=m_0$.

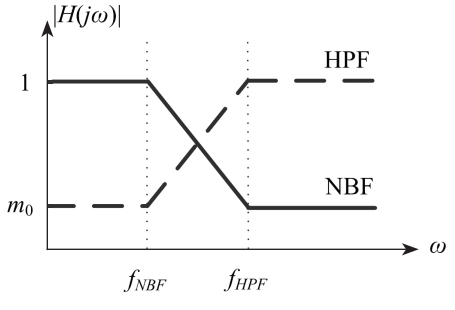


Fig. 3. Frequency response of the narrow-band filter and high-pass filter

Let us consider the principle of the modified PLL in the time domain on the example of the harmonic signal, which is sent to the device input.

Let us suppose the harmonic signal $s(t)=\sin(\omega t)$ is at the input, where ω is the input signal frequency, and the output quadrature signals of the modified PLL are $y_i(t)=\sin(\omega_0 t+\theta)$ and $y_q(t)=\cos(\omega_0 t+\theta)$, where ω_0 and θ are the frequency and phase of the reference oscillator (RO). Then, quadrature signals are received after narrowband filtration in the NBF:

$$v_{NBFi}=\frac{1}{2}\sin(\Delta\omega t-\theta)+\frac{m_0}{2}\sin(2\omega_0 t+\Delta\omega t+\theta), \quad (3)$$

$$v_{NBFq}=\frac{1}{2}\cos(\Delta\omega t-\theta)+\frac{m_0}{2}\sin(2\omega_0 t+\Delta\omega t+\theta), \quad (4)$$

where $\Delta\omega=\omega-\omega_0$.

After the inverse transfer of the spectrum to the carrier frequency, we receive the filtered signals:

$$s_{NBFi}(t)=\frac{1}{4}\left[\begin{matrix}(1+m_0)\sin(\omega t)-\sin(\omega_0 t-\Delta\omega t+2\theta)+\\+m_0\sin(3\omega_0 t+\Delta\omega t+2\theta)\end{matrix}\right], \quad (5)$$

$$s_{NBFq}(t)=\frac{1}{4}\left[\begin{matrix}(1+m_0)\sin(\omega t)+\sin(\omega_0 t-\Delta\omega t+2\theta)-\\-m_0\sin(3\omega_0 t+\Delta\omega t+2\theta)\end{matrix}\right]. \quad (6)$$

Thus, the full signal at the *NBF* output is described by the expression:

$$s_{NBF}(t)=\frac{1+m_0}{4}\sin(\omega t). \quad (7)$$

So the *NBF* gain equals:

$$K_{NBF}=\frac{1+m_0}{4}. \quad (8)$$

At the PD output, the signal has a low-frequency and high-frequency component and it is described by the expression:

$$v(t)=\frac{1+m_0}{4}\left[\sin(\Delta\omega t-\theta)-\sin(2\omega_0 t+\Delta\omega t+\theta)\right]. \quad (9)$$

Both components pass through filters: low frequency is suppressed $1/m_0$ times, and high frequency $-1/m$ times. So the error signal of the device is described by the expression:

$$e(t)=\frac{1+m_0}{4}\left[\begin{matrix}m_0\cdot\sin(\Delta\omega t-\theta)-\\-m\cdot\sin(2\omega_0 t+\Delta\omega t+\theta)\end{matrix}\right]. \quad (10)$$

Using the multiversion calculations according to the expression (10), a large amount of numerical data is obtained and the generalized results of their analysis are given below.

Firstly, the gain of the modified device is smaller than in the classical one (in case of their identical parameters) $(1+m_0)/4$ times. In addition, the desired low-frequency component of the error signal is also smaller than that in the classical one ($1/m_0$ times), because the summary frequency response of NBF and HPF is $K_{NBF}(s)K_{HPF}(s)=m_0$. Therefore, for further experiments of comparison of the noise immunity of both devices, it is necessary to bring an additional factor $(1+m_0)/4m_0$ in the modified PLL to compensate for this effect. And finally, the double frequency component filtration at the LPF output in the modified PLL is worse. To minimize this effect, it is necessary to choose the largest possible carrier frequency and also increase the ratio m_0/m.

4. 3. Hardware and software parts of the modified PLL

Classical and modified variants of PLL are implemented using the Cmod A7-35T development board, based on the Artix-7 architecture of the programmable logic integrated

circuit (FPGA) of American corporation Xilinx [21]. This board was chosen because the resources of standard microcontrollers may not be sufficient to process signals with frequencies of tens of kilohertz and higher, and more productive microcontrollers and digital signal processors (DSP) are much more expensive. At the same time, FPGA is a great tool for high-speed digital signal processing, and this board is one of the cheapest. In addition, with the ability to perform many operations in the FPGA in parallel, it is easier to develop a mechanism for controlling the PLL parameters and generate additional signals for their research.

In addition to the FPGA chip itself, both devices include 12-bit ADCs (AD7274) and DACs (AD5449) and adder built on the basis of AD8615 op amp (Fig. 4). Since the FPGA programming process is quite time-consuming, a mechanism for data exchange with a personal computer (PC) in order to change PLL parameters in real time and monitor the parameters of input and output signals was implemented. It is also possible to specify the type of PLL device (classical or modified) from the PC, which is being investigated at the moment.

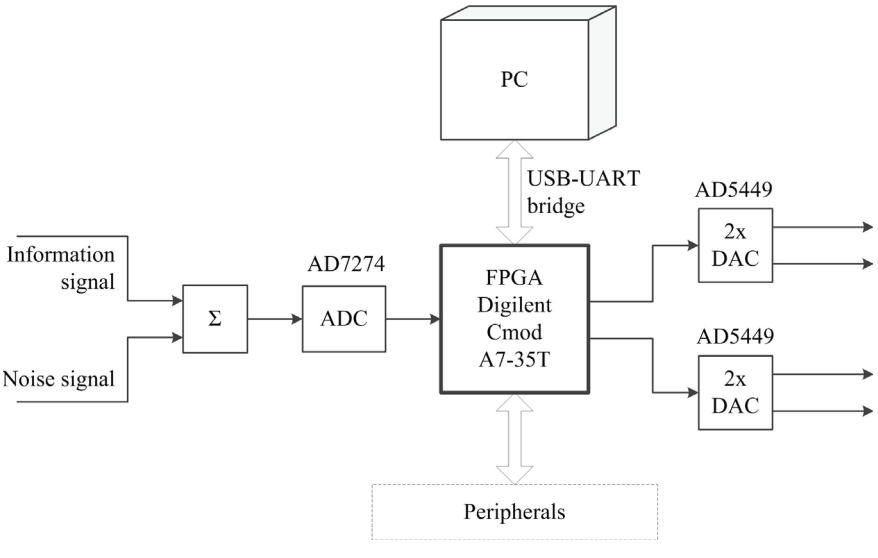


Fig. 4. Block diagram of software implementation of the PLL

The software for the device is developed in Xilinx Vivado 2017.2, and the interface between PC and FPGA – in MATLAB. Using the program in MATLAB, it is possible to specify the parameters of each component of the device and the type of the investigated device (classical or modified) and determine the list of signals for observation on the oscilloscope.

5. Method and criteria of noise immunity simulation

5. 1. Selection of classical and modified PLL parameters

The experiment was carried out for three sets of parameters that differ in a PLL closed loop gain (Fs – sampling rate) to perform simulation:

1) $K_1=K_{01}K_{PD}=2{,}500\ s^{-1}$;

$f_{c1}=25$ Hz; $m_1=0.0025$; $f_{HPF1}=100$ Hz; $F_s=100$ kHz.

2) $K_2=K_{02}K_{PD}=5{,}000\ s^{-1}$;

$f_{c2}=50$ Hz; $m_2=0.005$; $f_{HPF2}=200$ Hz; $F_s=100$ kHz.

3) $K_3=K_{03}K_{PD}=10{,}000\ s^{-1}$;

$f_{c3}=100$ Hz; $m_3=0.01$; $f_{HPF3}=500$ Hz; $F_s=100$ kHz.

For each of the three sets, a detailed selection of m_0 values in the range from 0.01 to 0.2 was performed. The cutoff frequency of the NBF was determined by the expression: $f_{NBF}=f_{HPF}m_0$.

These sets of parameters were chosen to analyze an influence of the NBF parameters on the device noise immunity. In addition, a wide set of parameters makes it possible to check whether holding ranges of classical and modified PLL match with each other. After all, the comparison of the noise immunity of both devices with different holding ranges is meaningless.

At the input of the device, an additive mixture of random noise (white noise) harmonic signal with a frequency $f=f_0+\Delta f$, where $f_0=5$ kHz is the center frequency of the DCO of the PLL, and $\Delta f=0.2f_{hold}$ is the initial frequency offset at the level of 20 % of the value of the device holding range f_{hold} was fed.

5. 2. Estimation of the noise immunity gain by the criterion of the average time between the output phase cycle slips

The first task was to find the noise threshold – the limiting value of the SNR, at which the synchronization breakdown occurs for both devices. There are a few different criteria for synchronization breakdown to be considered.

According to the first criterion, the loss of synchronization occurs with a quick increase in the number of phase cycle slips at the DCO output, when the average time between phase cycle slips becomes comparable with the duration of the transient process of establishing synchronization. In order to estimate the noise threshold for this criterion, an experiment was conducted, the essence of which is as follows.

There is a mixture of harmonic signal and random interference at the device input. In this case, at some moments of time at the DCO output, abnormal phase jumps at a value of 2π will be observed (Fig. 5), which means that the PD of the device cannot trace the change of the information signal phase and skipped its one period. By observing this signal over a long time interval, it is possible to estimate an average number of these anomalous jumps per second for different SNR values at the device input by observing this signal over a long time interval.

Fig. 5 indicates the results of the classical and modified devices simulation for two values of SNR. Fig. 5, *a* shows that at a low noise power level (SNR=2.5 dB), the modified PLL keeps synchronization without any phase slip, whereas in the classical device, there are occasional abnormal jumps, the frequency of which, however, is small.

Fig. 5, *b* shows that at a higher intensity of noise (SNR=0 dB), phase jumps occur in both devices. However, in the classical PLL, they occur much more often than in the modified one, which indicates better noise immunity of the latter.

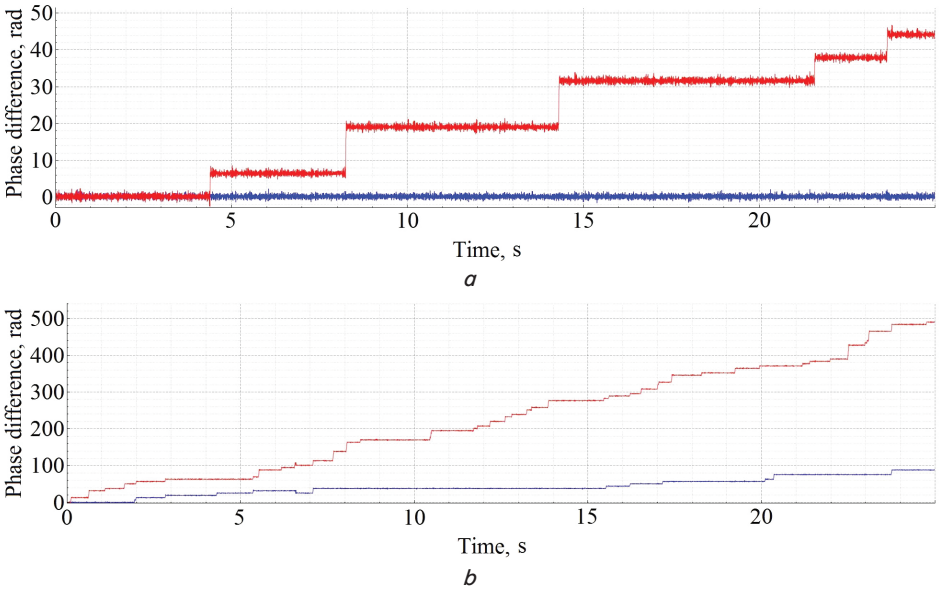


Fig. 5. Dynamics of the phase difference change between the input and output signals in time at fixed SNR: *a* – SNR=2.5 dB, *b* – SNR=0 dB. The red line of the graph corresponds to the classical PLL, blue – to the modified PLL

To summarize the results into an integral picture, a series of simulation experiments were conducted for different values of the SNR and sets of the classical and modified device parameters. The results of the simulation are presented in Fig. 6, which depicts plots of the average time between the phase cycle slips depending on the SNR value.

Plots in Fig. 6 show that multiple cycle slips for a short time intervals are observed at lower noise levels for the classical PLL device, and at higher noise levels for the modified PLL. Thus, the results of the noise immunity comparison for this criterion also show a decrease in the noise threshold of the PLL. For $m_0>0.1$, the improvement is 1.5–2 dB, and 3–4 dB for $m_0<0.1$.

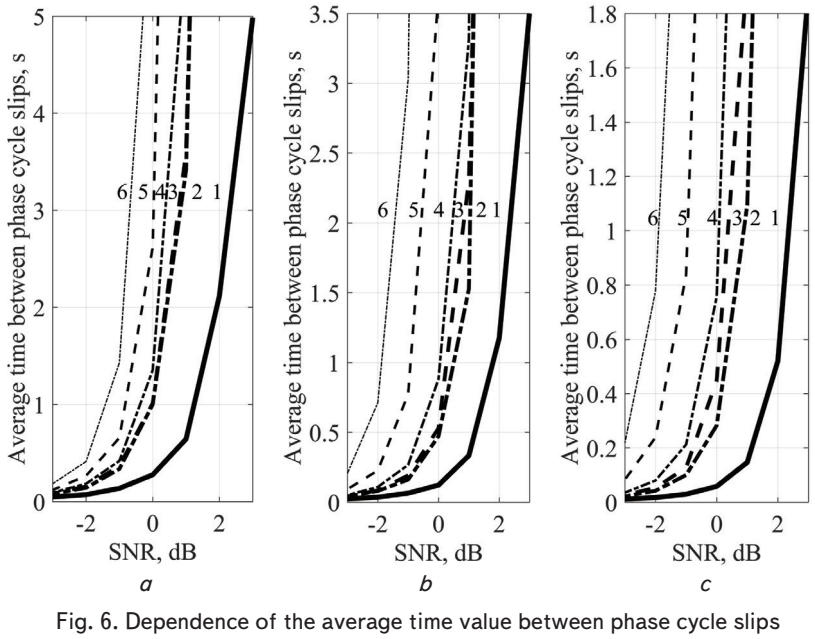


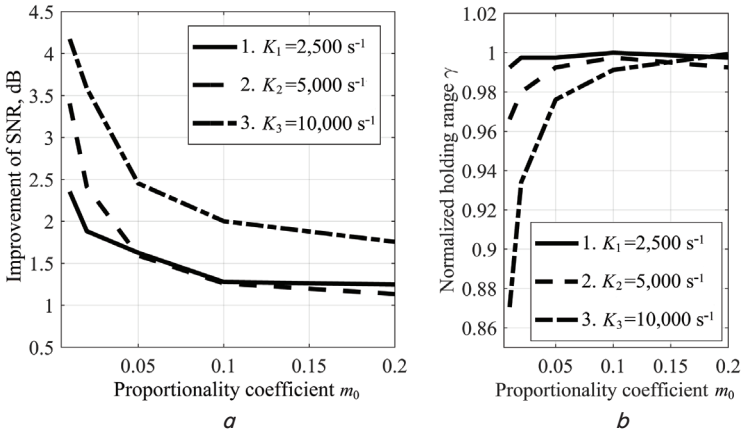
Fig. 6. Dependence of the average time value between phase cycle slips on SNR for a series of the NBF proportionality coefficient values m_0 (1 – $m_0=1$, the classical device; 2 – $m_0=0.2$; 3 – $m_0=0.1$; 4 – $m_0=0$; 05; 5 – $m_0=0.02$; 6 – $m_0=0.01$) and three parameters of the modified device K_1, K_2, K_3: *a* – $K_1=2{,}500\ s^{-1}$, *b* – $K_2=5{,}000\ s^{-1}$; *c* – $K_3=10{,}000\ s^{-1}$

5. 3. Estimation of the noise immunity gain by the criterion of the first phase cycle slip of the output signal

According to another criterion, the noise threshold is considered to be the value of the SNR, at which the first cycle slip of the DCO phase is observed for the value of 2π. In this case, the experiment of noise immunity research is practically identical to the previous one with the difference that the power of the random noise signal gradually increases with time linearly. Accordingly, if the time from the beginning of the simulation, when an abnormal phase step at the DCO output occurs, is fixed, then it is possible to determine the power of noise with high accuracy, and therefore – the critical value of the SNR, which causes synchronization loss of the PLL.

The simulation of the noise immunity of classical and modified devices by this criterion was performed for several NBF parameters m_0 and the loop gain K of the device. The simulation results are shown in Fig. 7 on the left. The simulation shows that use of the modified device provides an improvement in the threshold SNR value by at least 1 dB (at $m_0=0.2$), and in case of large holding range and a small value of the NBF proportionality coefficient – up to 4 dB (at $m_0=0.01$ and $K=20{,}000$).

An essential condition for an adequate comparison of noise immunity is the equality of holding ranges of both devices in the static mode without external noise signals. Therefore, in order to determine whether the change of the NBF parameters of the modified device influences its holding range, an additional experiment was carried out, the results of which are shown in Fig. 7 on the right. The results of the experiment are presented in the form of plots of the modified device normalized holding range (relative to the classical one) dependence on the parameter m_0 of the NBF and the PLL loop gain K.



a *b*

Fig. 7. Influence of the NBF proportionality coefficient for various PLL loop gains K on: *a* – improvement of the modified device noise immunity, and *b* – holding range of the modified PLL

The results of the additional experiment indicate that for small coefficients of K, when the absolute value of the PLL holding range is small, the change of the proportionality coefficient does not affect the change of the modified PLL holding range. However, with an increase of the coefficient K for small values of $m_0 \leq 0.01$, there is a significant decrease of the holding range (deviation exceeds 5 % of the nominal value).

The difference in improvement of the noise immunity is not steady because of the statistical nature of noise, so when the PLL behavior is simulated for the same value of parameters, the result will be somewhat different each time. Fig. 6 depicts the results of averaging 100 experiments for each set of parameters, which provides a mean square deviation of the results up to 1.5 dB.

6. Results of experimental research of noise immunity

6. 1. Experimental comparison of noise thresholds of classical and modified PLL

An experimental research of the PLL noise immunity was conducted for the same parameters of the device. The results of the experiments are shown in Fig. 8.

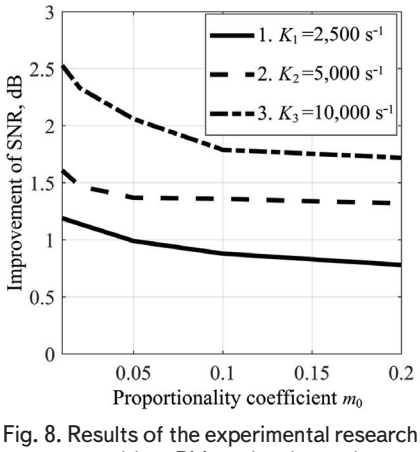


Fig. 8. Results of the experimental research of the modified PLL noise immunity for three sets of parameters (1–3)

Plots in Fig. 8 show that a greater gain in the noise immunity of the PLL is observed at higher values of the device gain (K=10,000) and at lower values of the NBF proportionality coefficient (m_0=0.01) and reaches 2.5 dB. It was also found that the effect of the NBF proportionality coefficient on the noise immunity improvement is shown up at values of $m_0 \leq 0.1$. Otherwise, the noise threshold is determined more by the gain K of the PLL.

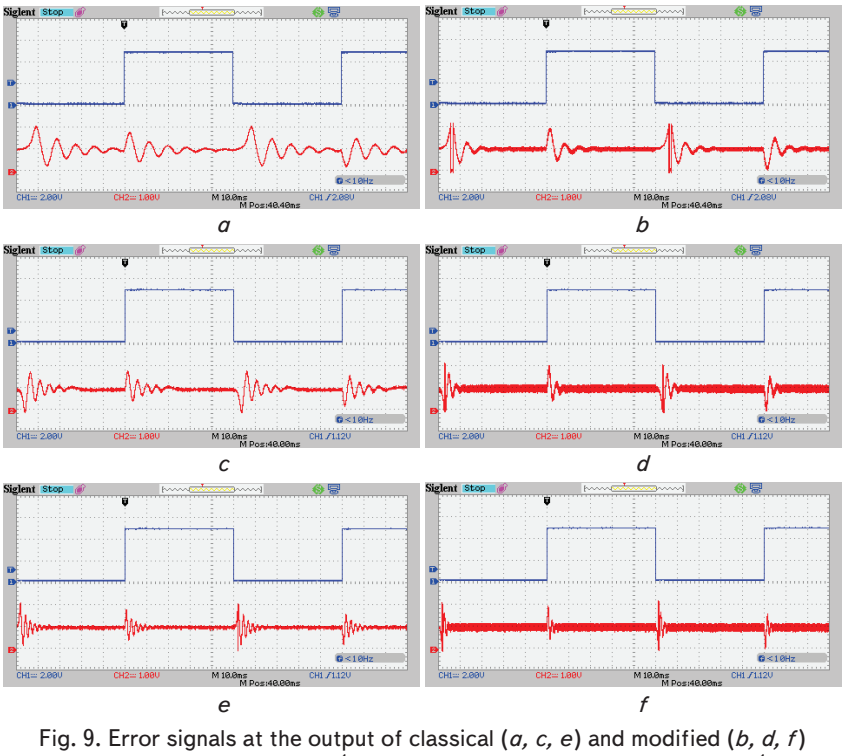
6. 2. Experimental study of dynamic properties of classical and modified PLL devices

To ensure that improvement of the modified PLL noise immunity did not cause a deterioration of its dynamic properties, a second experiment was conducted. A QPSK signal was sent to the device input at the reference carrier frequency without noise. The goal of the experiment was to compare output signals from the LPF of both devices.

If the dynamic properties of the modified PLL were worse than those of the classical one, then at the moments of the phase steps of the input oscillation, the error signal in the modified device would be delayed more than in the classical one.

For this purpose, an experiment, which was to fix the response of the classical and modified detector on the phase-manipulated signal was conducted. The results of the experiment are shown in Fig. 9.

Experimental results, presented in Fig. 9, show preservation and even improvement of dynamic characteristics. This effect was observed in versions of device implementation with different holding ranges. In all illustrated cases, the duration of the transient process to the establishment of a constant phase value at the DCO output in the modified device was reduced approximately 1.5 times.



a *b* *c* *d* *e* *f*

Fig. 9. Error signals at the output of classical (*a, c, e*) and modified (*b, d, f*) devices: *a* – K_1=2,500 s^{-1}; *b* – K_1 and m_0=0.05; *c* – K_2=5,000 s^{-1}; *d* – K_2 and m_0=0.1; *e* – K_3=10,000 s^{-1}; *f* – K_3 and m_0=0.2

7. Discussion of the design, simulation and experiments results

At first glance, achieving a greater improvement in the noise immunity of the modified device consists in reducing the parameter of NBF m_0 and the device gain K. It has been found that under $m_0 < m$ such changes cause significant nonlinear distortions of the output signal, because the harmonic for the double frequency at the detector output is almost not filtered. As a result, the static characteristic of the device loses its symmetry, and the holding range becomes less than the nominal value [22].

Another reason, which causes a decrease of the modified PLL holding range is that the formula (8) for calculating the NBF transfer function is approximate, because it does not take into account nonlinear effects during the change of the input signal frequency. If the cutoff frequency of the NBF is comparable with units of Hertz (or even less), then even the smallest change in the input signal frequency will trigger a change in the NBF transfer function, and hence the transfer function of the entire device (which defines the holding range). The finding of the exact expression of the NBF transfer function requires additional analytical research.

Therefore, comparing the noise immunity of both devices with such parameters is not appropriate, because equal initial conditions of research are not ensured. It means that there is a certain optimal value of the parameter m_0 of the narrowband filter (in this case from 0.05 to 0.1), which allows a decent gain in noise immunity (up to 2.5 dB) and at the same time maintenance of the device static characteristic unchanged.

The results of the experimental research qualitatively correspond to the results of the simulation, because the nature of the dependence of the gain in the noise immunity on the parameters m_0 and K remains. From the quantitative point of view, the experiment shows a somewhat smaller gain in the noise immunity of the device (1–1.5 dB lower), which is explained by the additional internal noise of the generator and the interference of external disturbances in the circle of the device.

The use of a modified phase detector improves the dynamic characteristics of the PLL, but at the same time it has a side effect. The presence of the HPF, the purpose of which is to restore harmonics of the information signal suppressed by the NBF, deteriorates the filtration of the double frequency harmonic of the information signal at the PD output. Fig. 10 clearly shows that the DCO phase signal for the modified device is noisier than for the classical one. To reduce the influence of this negative effect, it is worth to increase the sampling rate, so that the ratio F_s/f_c is as high as possible and also to reduce the parameter m of the LPF to fulfil the condition $m_0 \gg m$.

8. Conclusions

1. Firmware implementation of the PLL on the FPGA platform was created, which ensured the improvement of its noise immunity with the preservation of dynamic properties. In addition, an interface for data exchange between a PC and the device was developed, which provided for quick changes of device parameters and type (classical or modified), which ensured the possibility to conduct experiments without multiple reprogramming of the device to change its parameters.

2. 3 sets of the PLL parameters, each of which has different holding range and NBF frequency responses were selected. The simulation of both devices for these three sets of parameters was performed to compare their noise thresholds. The comparison showed a noise immunity improvement of the modified device to 2 dB compared to the classical one with the NBF proportionality coefficient $m_0 > 0.1$. At $m_0 < 0.1$, improvement is even greater (up to 4 dB), but in this case the holding range of the modified device changes its value.

3. The experimental research of classical and modified devices for the same sets of parameters was conducted to compare their noise thresholds. The results of the experimental research qualitatively repeat the simulation results. The comparison shows that the noise threshold of the modified device is up to 2.5 dB lower than the threshold of the classical one.

4. Dynamic properties of classical and modified PLL devices were investigated by comparing the duration of the transient process at the DCO input at the moment of the information message change of the incoming QPSK signal. The comparison shows an opportunity to improve the dynamic properties 1.5 times with maintaining the level of noise threshold.

The results obtained in the work can be directly used to increase the capacity of existing communication systems. The results demonstrate the potential of communication systems operation under conditions of higher levels of noise, as well as the increment in the number of users who use the system simultaneously. The expected gain of the system capacity is 1.5–2 times.

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