

UDC 004.052

J. V. Drozd, PhD.,
M. A. Drozd

A RESOURCE APPROACH TO DEVELOPMENT OF THE GREEN TECHNOLOGIES IN COMPUTER SYSTEMS AND THEIR COMPONENTS

Abstract. The problem of limitation of the modern green technologies exploiting in computer systems only an idea of supply voltage reduction and based on diversification of hardware means and modes of their operation is considered. A resource approach to development of the green technologies is offered. The models, methods and means used for solving the challenges including the problems of both design and testing of the computer systems and their components belong to the resources. Development of the resources in direction of increasing the levels of both parallelism and fuzziness is shown. The methods supporting this direction for further development of the green technologies in computer systems are proposed.

Keywords: computer systems, green technologies, models, methods, large-scale and pipeline parallelism, safety-critical system, checkability

Ю. В. Дрозд, канд. техн. наук,
М. А. Дрозд

РЕСУРСНЫЙ ПОДХОД К РАЗВИТИЮ ЗЕЛЕННЫХ ТЕХНОЛОГИЙ В КОМПЬЮТЕРНЫХ СИСТЕМАХ И ИХ КОМПОНЕНТАХ

Аннотация. Рассматривается проблема ограниченности современных зеленых технологий, эксплуатирующих в компьютерных системах только идею снижения напряжения питания и базирующихся на диверсификации аппаратных средств и режимов их работы. Предлагается ресурсный подход к развитию зеленых технологий. К ресурсам отнесены модели, методы и средства, используемые для решения вызовов, включая проблемы проектирования и диагностирования компьютерных систем и их компонентов. Показано развитие ресурсов в направлении повышения уровня параллелизма и размытости. Предлагаются методы, поддерживающие это направление для дальнейшего развития зеленых технологий в компьютерных системах.

Ключевые слова: компьютерные системы, зеленые технологии, модели, методы, средства, матричный и конвейерный параллелизм, система критического применения, контролепригодность

Ю. В. Дрозд, канд. техн. наук,
М. О. Дрозд

РЕСУРСНИЙ ПІДХІД ДО РОЗВИТКУ ЗЕЛЕНИХ ТЕХНОЛОГІЙ В КОМП'ЮТЕРНИХ СИСТЕМАХ ТА ЇХ КОМПОНЕНТАХ

Анотація. Розглядається проблема обмеженості сучасних зелених технологій, що в комп'ютерних системах експлуатують лише ідею зниження напруги живлення та базуються на диверсифікації апаратних засобів і режимів їх роботи. Пропонується ресурсний підхід до розвитку зелених технологій. До ресурсів віднесено моделі, методи та засоби, що використовуються для розв'язання викликів, включаючи проблеми проектування й діагностування комп'ютерних систем та їх компонентів. Показано розвиток ресурсів у напрямку підвищення рівня паралелізму та розмитості. Пропонуються методи, що підтримують цей напрямок для подальшого розвитку зелених технологій в комп'ютерних системах.

Ключові слова: комп'ютерні системи, зелені технології, моделі, методи, засоби, матричний та конвеєрний паралелізм, системи критичного застосування, контролепридатність

Introduction. Analysis of green-oriented approaches to structure and operation of computer means controllers, processors a. o. shows that all these decisions exploits an idea of supply voltage reduction based on the formula of a dynamic part of the energy consumption $I_{DYN} = CV^2f$, where C – loading capacitance, V – supply voltage, f – clock frequency [1]. This idea is realized using concept of diversity applied to units and modes of their operation.

For example, energy saving technology AMD Cool'n'Quiet and Intel Enhanced SpeedStep proposed regular reduction of supply voltage and appropriate clock frequency [2].

The processors AMD Phenom and Phenom II can change these parameters for every core independently of the rest. The processor Exynos S Octa is completed by 4 cores Cortex-A7 with low energy consumption and 4 cores Cortex-A15 with high throughput using the technology ARM big.LITTLE for energy saving at the level of 70 % [3].

© Drozd J.V., Drozd M.A., 2013

Series of microcontrollers STM8L15x/162 ensures 5 modes of energy saving: Wait, Low power run, Low power wait, Active-halt and Halt [4].

Concept of diversity provides profiling of units and their operation modes under particularities of the solved tasks. Process of profiling leads to increase of expenses and reduction of benefits limiting development of modern green technologies.

Further development of the green technologies can be executed using resource approach considered in the following section.

Foundations of resource approach.

Development of the Computer World can be considered as process of solving the challenges, including problems in co-design and testing of computer systems.

The problem can be solved at performance of three conditions:

- execution of a set of works for limited time achieving the certain throughput;
- reception of reliable results;
- investment of the certain resources.

The resources contain all necessary for solving a problem: models, methods and means. Models are our ideas of the Universe and its components. Methods describe the transformations, which are carried out with resources. Means (materials and tools) allow realizing these transformations and verifying models and methods.

All resources as elements of our parallel and fuzzy Universe are structured under its features growing level of parallelism and approximate decisions in co-design and testing of computer systems and their components [5].

For example, the personal computers have passed a way from hardware support of approximate data processing in co-processors of non-obligatory delivery (Intel 8087/287/387) up to several floating-point pipelines in structure of the Pentium CPU and up to many thousand floating point pipelines in the graphic processor with execution of parallel calculations on technology CUDA [6].

Natural development of resources is stimulated by the method of carrot and stick. A stick is natural selection, and carrot is gifts for resource structurization under features of the Universe [7].

The personal computers raise clock frequency (throughput) from KHz up to GHz and at once increase size of memory from Mb up to Tb – in millions times during 20 last years. Other parameters are also improved many times including cost.

Offered approach is consisting in development of resources raising levels of parallelism, fuzziness and other features of the Universe.

Analysis of parallelism kinds shows that large-scale parallelism based on replication of the operational elements is allocated at the last place. It is the most resource-demanding. Process of large-scale paralleling can be limited by dependences on both data and control. However the modern computing units are built using large-scale parallelism realized in parallel adders, iterative array multipliers and dividers.

For example, an iterative array multiplier of two n -bit binary codes consists of $n^2 - n$ operational elements. Its critical way (for the best structure) contains $2n - 2$ operational elements. For $n = 32$ this way is equal to 62 allowing to operate every operational element only $1 / 62$ part of clock unit (1.6%). All of 992 operational elements stand idle 98.4% of operation time because of dependence on data.

We propose the methods of unit transformation from low levels up to high ones of adequacy to Universe.

For example, the method of multiplier transformation from unit with iterative array structure based on large-scale parallelism to decision with pipeline parallelism which is free from dependence on data. Large scale parallelism of pipeline stages is reduced down to minimum in case of bit-series data processing.

Time of repeated multiplication in iterative array unit and bit-series pipeline one are calculated by the following formulas:

$$T_{IA} = (2n - 2)t_{FA} + t_{AND} + t_R;$$

$$T_{BP} = 2n(t_{FA} + t_{AND}),$$

where t_{FA} is delay of full adder;

t_{AND} is delay of AND gate;

t_R is delay of register.

Let $T_{BP} = k_T T_{IA}$ and $t_{AND} + t_R = z t_{FA}$. Then

$$k_T = 2n(z + 1) / (2n - 2 + z).$$

For $z \geq 2$ throughput of iterative array multiplier is compensated with use of $k_T = z + 1$ bit-series pipeline unit. Such large-scale parallelism is free from data dependence.

Complexity of iterative array and bit-series pipeline units can be estimated as amount of both full adders and flip-flops by the following formulas: $C_{IA} = n^2 + n$; $C_{BP} = 6n$.

Ratio $k_C = C_{IA} / C_{BP} = (n+1)/6$ shows that in case of equal complexity pipeline decision increases throughput $K = k_C / k_T$ times.

For $z = 2$, $n = 32$, and $n = 64$ throughput increases $K = 1,8$ and $K = 3,6$ times accordingly. This benefit can be transformed into energy saving reducing supply voltage and clock frequency K times [1].

Reducing of supply voltage increases time of calculation at first linearly and then with square-law. Let time increases $H < K$ times linearly. It reduces energy consumption H^2 and K/H times at the linear and square periods accordingly and HK times total. In cases $H = 1,5$ and $H = K$ energy consumption is reduced 2.7 and 3.2 times for $n = 32$ and also 5.4 and 13 times for $n = 64$.

Use of the bit-series pipeline processing of data provides at once a set of other benefits including high level of checkability. This attribute plays important role in maintaining functionality for safety-critical instrumentation and control systems used for monitoring the objects of raised risk in power industry, transport, space and military areas [8].

Such systems can be related to two kinds in dependence on requirements to throughput of their digital components. The first kind including, for example, reactor-trip systems for nuclear power plants does not require high throughput because of inertia of control objects. The second kind contains special dedicated computing systems with high requirement to throughput for execution of large size of the calculations [7].

The main feature of safety-critical systems is their design for operation in two modes: normal and emergency. These systems are designed for emergency mode, but they run in the normal mode for most of operating time [9].

Now safety-critical systems have low checkability determined by the two reasons.

First, for safety the components of these systems should be fault tolerant. It is achieved using redundant structure which reduces checkability [10].

Second, the digital components work in both modes on the different limited sets of input words. Traditional design of these components like simultaneous fault tolerant units with large-scale parallelism determines low level of data changing and additionally reduces checkability/It leads in normal mode to accumulation of latent faults breaking functionality of system in an emergency mode [11].

In testing the checkability of a component digital circuit is determined using two properties: controllability and observability of the circuit points [12].

For on-line testing the checkability is identify with observability, and controllability is high bound of it [7].

The use of bit-series pipeline unit makes all circuit points controllable as well as they change values on non-zero direct or inverse code. Observability of circuit points approaches to its high bound due logic function of XOR executed in the full adder which is the main element of the computing units. Additionally observability of the digital circuits can be increased by using of extra check points.

Array of the bit-series pipeline units allows supporting required levels of data processing in throughput, fault tolerance and checkability simultaneously.

Conclusions. Modern green technologies are limited by possibilities of profiling the hardware means and modes under particularities of the solved tasks. Offered resource approach opens way for development of the green technologies take into account benefits of raising levels of adequacy to features of Universe and firs of all its parallelism.

Transformation of the simultaneous units with large-scale parallelism into array of bit-series pipeline ones allows at once to improve a set of attributes including throughput, fault tolerance and checkability. It is very important for maintaining functionality of the safety-critical instrumentation and control systems.

References

1. Chandracasan A.P., Sheng R., and Brodersen S. Low-Power CMOS Digital Design, (1992), *IEEE Journal of Solid-State Circuits Publ.*, Vol. 27, No. 4, pp. 473 – 484 (In English).
2. Cool'n'Quiet™ Technology Installation Guide for AMD Athlon™ 64 Processor Based Systems [2004 Advanced Micro Devices, Inc] (In English), url: http://web.archive.org/web/20070409045621/http://www.amd.com/us-en/assets/content_type/DownloadableAssets/Cool_N_Quiet_Installation_Guide3.pdf.
3. Michael Larabel Intel EIST SpeedStep (16.02.2006). [Phoronix] (In English), url: <http://www.phoronix.com/scan.php?page=article&item=397&num=1>.
4. STMicroelectronics STM8L Family Power Management (15.03.2010) [AN3147] (In English), url: <http://www.bdtic.com/DownLoad/ST/AN3147.pdf>.
5. Drozd J., and Drozd A. Models, Methods and Means for Solving the Challenges in Co-Design and Testing of Computer Systems and their Components, (2013), *Reliability: Theory & Applications Publ.*, San Diego, USA, Vol. 8, No 4, (31), pp. 66 – 74 (In English).
6. NVIDIA CUDA Compute Unified Device Architecture, Programming Guide, (2007), *Version 1.0, NVIDIA Corporation* (In English).
7. Drozd A.V., Kharchenko V.S. (edits). On-line Testing of the Safe Instrumentation and Control Systems, (2012), Kharkiv, Ukraine, *National Aerospace University named after N.E. Zhukovsky "KhAI"*, 614 p. (In Russian).
8. Kharchenko V.S., Sklyar V.V. (edits). FPGA-based NPP I&C Systems: Development and Safety Assessment, (2008), Kirovograd, Ukraine, *RPC Radiy, Kharkov, Ukraine, National Aerospace University named after N.E. Zhukovsky "KhAI", SSTC on Nuclear and Radiation Safety*, 188 p. (In English).
9. Drozd A., Kharchenko V., Antoshchuk S., Sulima J. and Drozd M. Checkability of the Digital Components in Safety-critical systems: Problems and Solutions, (2011), *Proc. IEEE East-West Design & Test Symposium Publ.*, Sevastopol, Ukraine, 9 – 12 Sept., pp. 411 – 416 (In English).
10. Goldstein G. Controllability. Observability analysis of digital circuits, (1979), *IEEE Trans. on Circuits and Systems Publ.*, No 9, pp. 685 – 693 (In English).
11. Drozd A., Kharchenko V., Antoshchuk S., and Drozd M. Checkability of safety-critical I&C system components in normal and emergency modes, (2012), *Journal of Information Control and Management Systems Publ.*, Vol. 10, No.1, pp. 33 – 40 (In English).
12. Bennets R.G., and Scott R.V. Recent developments in the theory and practice of testable logic design, (1977), *IEEE Comput Publ.*, Vol. 9, No. 6, pp. 47 – 63 (In English).

Received 15.10.2013



Drozd Julia V.
Associate Professor of
Information Systems
Department, Odessa
National Polytechnic
University, Shevchenko
ave. 1, Odessa, Ukraine,
65044.
E-mail: dea_lucis@ukr.net



Drozd Miroslav A.
Postgraduate Student of
Information Systems,
Odessa National
Polytechnic University,
Shevchenko ave. 1,
Odessa, Ukraine, 65044.
E-mail: drozd@ukr.net