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ESTIMATION OF POWER CONSUMPTION DISTRIBUTION IN FPGA-PROJECTS

Abstract. *Green-orientation of modern CAD systems based on Altera Quartus II and build-in utility PowerPlay Power Analyzer, allowing to optimize and to estimate FPGA-project by power consumption within the scope of signal activity management is regarded in this paper. Set of experiments show the importance of optimizing FPGA-project with its actual signals activity. Method for estimation of FPGA-project's dynamic power consumption component distribution between parts of its scheme is offered. Method determines contribution of separate parts of the scheme to project's power consumption by lowering signals activity, common for other parts of the scheme, for example, clock signals.*

Keywords: *computer systems, green technologies, models, methods, large-scale and pipeline parallelism, safety-critical system, checkability*

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ОЦЕНКА РАСПРЕДЕЛЕНИЯ ЭНЕРГОПОТРЕБЛЕНИЯ В FPGA ПРОЕКТЕ

Аннотация. *Рассматривается грин–ориентация современных САПР на примере Altera Quartus II и встроенной в нее утилиты «PowerPlay Power Analyzer Tool», позволяющей оптимизировать и оценивать FPGA-проекты по энергопотреблению с учетом активности сигналов схемы. На серии экспериментов показывается важность оптимизации FPGA-проекта при реальной активности сигналов. Предлагается метод оценки FPGA-проекта в распределении динамической составляющей энергопотребления между частями его схемы. Метод определяет вклад отдельных частей схемы в энергопотребление FPGA-проекта путем снижения активности сигналов, общих для остальных частей схемы, например, тактирующих сигналов.*

Ключевые слова: *компьютерные системы, цифровая схема, грин–технологии, FPGA-проект, оптимизация и оценка энергопотребления, активность сигналов*

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ОЦІНКА РОЗПОДІЛЕННЯ ЕНЕРГОСПОЖИВАННЯ В FPGA ПРОЕКТІ

Анотація. *Розглядається грин-орієнтація сучасних САПР на прикладі Altera Quartus II та вбудованої до неї утиліти «PowerPlay Power Analyzer Tool», що дозволяє оптимізувати та оцінити FPGA-проекти по енергоспоживанню з урахуванням активності сигналів схеми. Серією експериментів ілюструється важливість оптимізації FPGA-проекту при реальній активності сигналів. Пропонується метод оцінки FPGA-проекту у розподіленні динамічної складової енергоспоживання між частинами його схеми. Метод визначає внесок окремих частин схеми у енергоспоживання FPGA-проекту шляхом зниження активності сигналів, загальних для інших частин схеми, наприклад, сигналів такту.*

Ключові слова: *комп'ютерні системи, зелені технології, моделі, методи, засоби, матричний та конвеєрний паралелізм, системи критичного застосування, активність сигналів*

Introduction

Green hardware decisions occupy a special place in development of computer systems and their components, implementing a general orientation towards energy saving as well as a necessary condition of low power consumption in improvement of autonomous and, in particular, mobile systems [1 – 3].

Modern design of digital units is executed with use of programmable logic devices in form of FPGA-projects supported by green-oriented CAD [4, 5].

For work with wide-used CPLD of company Altera the CAD Quartus II [6, 7] is used. This system has embedded utility «PowerPlay Power Analyzer Tool», hereinafter referred to as PowerPlay, which allows developing and estimating an FPGA-project taking into account power consumption [8 – 11].

The static and dynamic constituents of power consumption are calculated for internal elements and outputs of the scheme. Power consumption is represented by current, expressed in milliamps subject to constant voltage. These indicators are integral for entire FPGA-project, leaving unanswered the question of distribution of power consumption inside the

scheme solution that can be used for correction of the most power intensive parts of the scheme. First of all, this drawback relates to estimations of the most significant dynamic constituents of power consumption of FPGA-project, which depend on scheme signal activity. The utility PowerPlay supply a variety of modes of setting the signal activity for optimization and estimation of power consumption. It is proposed a series of experiments, demonstrating the importance of adaptation of FPGA-project to real signal activity, and also the method of estimation of FPGA-project by distribution of power consumption between the separate parts of its schemes.

Signal activity account on the stage of project optimization

Optimization of FPGA-project allows taking into consideration the scheme signal activity. For this there is provided the creation of a Signal Activity File (SAF), where for each signal there is defined the pattern of toggles using two parameters: toggle rate – the average number of times that the signal changes value per unit of time, and static probability – the fraction of time that the signal is logic 1 during the period of device operation that is being analyzed.

In estimation of power consumption of FPGA-project also can be considered the signal activity using the same or another SAF.

The importance of adaptation of FPGA-project to real signal activity is demonstrated by the experiments, where the same and different signal activity is the set for optimization and estimation of power consumption.

The analyzed scheme writes three 64-bit codewords A, B и C, into three 64-bit registers [10]. At the output of the registers the sum A + B is compared with codeword C. The scheme is designed in system Quartus II 13.0.0.32-bit for device EP2C35F672C6.

For this project are created two SAF:

- SAF 1 contains the default values of signals activity, (all input signals have toggle rate $5*10^7$ and static probability 0,5);
- The difference between SAF 2 and SAF 1 is, that toggle rate of the input codeword C equals zero, and i.e. all signals of the codeword C are constant.

The power consumption of the scheme is measured in four experiments using the utility Power Play.

Experiment 1: for optimization and estimation of power consumption of the scheme is used the same file SAF 1.

Experiment 2: for optimization is used SAF 1, for estimation – SAF 2 with less number of toggles.

Experiment 3: for optimization is used SAF 2, for estimation – SAF 1 with bigger number of toggles.

Experiment 4: for optimization and estimation is used the same file SAF 2 with less number of toggles in comparison with experiment 1.

The results of these experiments are shown in table 1.

1. The results of the experiments

No.	V_{CC}	I_D, mA	I_S, mA	I, mA
1	INT	45,59	79,40	124,99
	IO	7,23	11,56	18,79
2	INT	42,79	79,14	121,93
	IO	4,58	11,56	16,14
3	INT	50,52	79,19	129,71
	IO	6,97	11,56	18,53
4	INT	35,46	79,34	114,80
	IO	4,95	11,56	16,51

In columns left to right there are shown the numbers of experiments 1 – 4, type of V_{CC} power (internal scheme elements INT or the outputs IO), currents I_D, I_S, I of dynamic and static constituents and their sum.

According to the results of experiments, the dynamic constituent of consumption is lower in cases, when for estimation is used SAF 2, setting the constant value to the bus C.

Comparison of results, obtained in the pairs of experiments 1, 3 and 2, 4 shows, that using the same file for optimization and power estimation, reduces the dynamic constituent by 10 – 20 %.

The benefit from power optimization significantly depends on conformity between the set signal activity and the real one during the scheme operation.

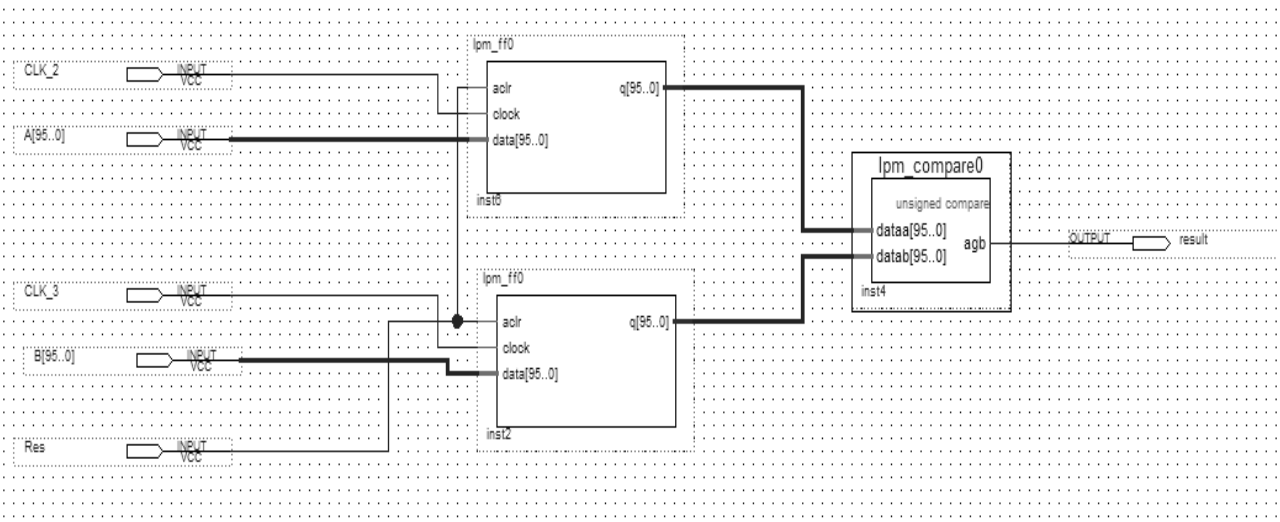

Fig. 1. Scheme designed for capacity n = 96

Accuracy of estimation of the dynamic constituent of consumption in FPGA-project increases when the data written in SAF is approaching to the real signal activity.

Estimation of FPGA-project in distribution of dynamic power consumption component between parts of the scheme

It is offered to estimate the contribution of separate scheme parts to the FPGA-project dynamic power consumption component by maximally reducing its signals activity in other:

– parts of the scheme. Such reducing is further called as *switching off*. It can be done by using;

– signals which are common for functionality of that scheme parts (for example clock or reset signals).

The task of FPGA-project estimation and its solution is illustrated by the next experiment, done with alteration of clock signals.

Experiment's initial conditions

In the capacity of researched scheme it was chosen one containing 2 *n*-sized registers RG A, RG B and comparator, taken from Quartus II default elements library. Informational inputs of registers are accordingly connected to inputs of scheme's n-sized binary codes A and B, and outputs – to comparatop inputs, which output is scheme's output. Clock inputs of registers RG A and RG B are connected accordingly to scheme's clock inputs CLK1 and CLK2, on which "meander-like" clock signals of same frequency of 400 MHz are given. On the clock signals codes A and B are accepted into registers and are compared on comparator, forming signal-digit comparing result at the scheme output.

The scheme is realized on 12 FPGA-projects, differing from each other by capacity *n* which accepts 12 different values: from *n* = 8 with the step of 8 to *n* = 96. The scheme is designed in CAD Altera Quartus II 13.0 Web Edition (64-bit version) on the chip EP2C35F672C6.

In Fig. 1 the scheme designed for capacity of *n* = 96 is shown.

Process of the experiment

The activity of signals is regulated in compiled and fitted on chip FPGA-project by bringing into it the SAF, containing the description of switching of clock signals activity on scheme's clock inputs CLK1 and CLK2. The process of switching off part of the scheme, clocked by CLK-signal, is made by setting this signal into constant value with zero toggle rates.

In experiment for each capacity *n* four variants of scheme's signals activity are specified, providing switching off for each part of the scheme: only register RG B, only register RG A and scheme's operation without switching off. All these variants are shown in Fig. 2 in pt. a – d accordingly.

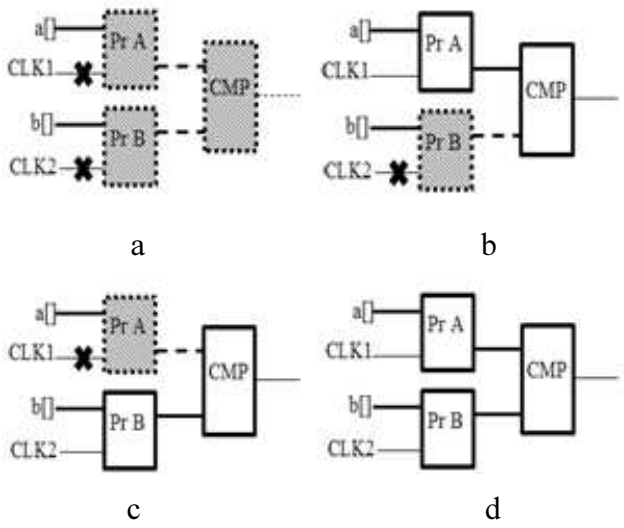

Fig. 2. The essence of the experiment:
a – switched off both registers; b – switched off register RG B; c – switched off register RG A; d – scheme is working without switching off

The estimation results for dynamic current strength on chip, taking on the value of I_{E1}, I_{E2}, I_{E3} and I_{E4} according to examined variants are shown in table 2.

2. Estimation results for dynamic current strength

No.	*n*	I_{E1}, *mA*	I_{E2}, *mA*	I_{E3}, *mA*	I_{E4}, *mA*
1	8	1,46	12,12	12,19	22,78
2	16	3,54	21,35	14,77	32,46
3	24	3,40	15,74	14,73	26,96
4	32	6,38	18,31	24,12	35,90
5	40	9,36	22,16	21,77	34,41
6	48	10,51	29,92	23,44	42,69
7	56	11,15	25,36	25,15	39,20
8	64	13,93	27,94	28,24	42,04
9	72	18,53	39,99	33,59	54,80
10	80	19,17	34,19	34,76	49,54
11	88	18,49	44,55	38,08	63,94
12	96	21,70	38,66	38,69	55,41

Results of experiment show that there is a stable persisting nonzero dynamic current strength component $I_0 = I_{E1}$ when all scheme's parts are switched off, increasing with the growth of capacity *n*.

Obtained results allow to calculate the power consumption of two parts of the scheme: register RG A and register RG B, estimated by current strengths $I_{RG\,A}$ and $I_{RG\,B}$ accordingly, by using next equations:

$$\begin{aligned} I_{E1} &= I_{0,} \\ I_{E2} &= I_0 + I_{RG\,A,} \\ I_{E3} &= I_0 + I_{RG\,B,} \end{aligned} \qquad (1)$$

hence

$$\begin{aligned} I_{RG\,A} &= I_{E2} - I_{E1,} \\ I_{RG\,B} &= I_{E3} - I_{E1}. \end{aligned} \qquad (2)$$

In addition, full scheme's power consumption represented by current I_T and relative estimation error of power consumption distribution between parts of the scheme are calculated:

$$\begin{aligned} I_T &= I_0 + I_{RG\,A} + I_{RG\,B}, \\ \Delta I &= \left| I_{E4} - I_T \right| / I_{E4}. \end{aligned} \qquad (3)$$

Results of calculations are shown in table 3.

3. Results of calculation

No.	*n*	I_0, *mA*	$I_{RG\,A}$, *mA*	$I_{RG\,B}$, *mA*	I_T, *mA*
1	8	1,46	10,66	10,73	22,85
2	16	3,54	17,81	11,23	32,58
3	24	3,40	12,34	11,33	27,07
4	32	6,38	11,93	17,74	36,05
5	40	9,36	12,8	12,41	34,57
6	48	10,51	19,41	12,93	42,85
7	56	11,15	14,21	14	39,36
8	64	13,93	14,01	14,31	42,25
9	72	18,53	21,46	15,06	55,05
10	80	19,17	15,02	15,59	49,78
11	88	18,49	26,06	19,59	64,14
12	96	21,70	16,96	16,99	55,65

For each capacity the relative error lies within the border 0,3 % – 0,5 %, which is below than maximal relative error of PowerPlay utility of 5 %.

It's important to add that in spite of full symmetry of the scheme, for some capacity registers show different values of power consumption, varying, as a rule, on 6 mA.

Conclusions

Experiments with signals activity management show their considerable influence on

FPGA-project power consumption optimization and its adaptation to real signals activity. In addition, signals activity management allows to estimate separate scheme parts contribution to power consumption of FPGA-project with high precision.

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