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COMPUTER AIDED DESIGN OF SINGLE-ELECTRON NANOCIRCUITS

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Abstract. *In this work proposed structure of field-programmable gate array based on five input majority gate.*

Keywords: nanoelectronics; single-electron circuits; logic gates; majority gate.

Introduction

Single-electron tunneling (SET) devices exploit effects that arise due to the quantized nature of charge. Therefore, single-electrons technology deals with the control of transport and position of a single or a small number of electrons. The fundamental physical principle of single-electronics is the tunneling effect through a Coulomb blockade, which has been observed and studied [1]. The small size and low power dissipation of SET circuits makes them potentially useful for logic and memory circuits. Several single-electron circuits have been recently proposed in the literature: single-electron memories [2], inverters [3], pumps [4], majority gates and logic gates [3]. A single-electron half-adder based on pass-transistor logic has been demonstrated. The need for computer-aided design and simulation of single-electron circuits has long been recognized [5]. Several simulators have been implemented to support single-electron circuit design [6]. The formatter will need to create these components, incorporating the applicable criteria that follow.

Single-electron circuits

Single-electron circuits consist of conducting islands, tunnel junctions, capacitors, and voltage sources. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. The basic principle of single electronics is that one needs Coulomb energy E_C to charge an island with an electron. This energy is:

$$E_C = \frac{e^2}{2C_i}, \tag{1}$$

where C_i is the total capacitance by the island and e – the elementary charge. Electrons tunnel independently from island to island through tunnel junctions. To assure that electron states are localized on islands all tunnel resistances must be bigger than the fundamental quantum resistance R_q:

$$R_T > R_q = \frac{h}{e^z} \cong 25813\Omega, \tag{2}$$

where h is Planck's constant.

To simulate the tunneling of electrons from island to island in a single-electron circuit, one has to determine the rates of all possible tunnel events. The tunnel rate of a possible tunnel event depends on the change in the circuit's free energy caused by this particular event. The free energy, F, of a single-electron circuit is the difference of the electrostatic energy, U, stored in its capacitances and the work done by the voltage sources of the circuit, W:

$$F = U - W. \tag{3}$$

The electrostatic energy is given by

$$U = \frac{1}{2}(q,V)\left(\frac{V}{Q}\right), \tag{4}$$

where, q and V are the unknown parts of the island charge and voltage matrices, respectively, and Q and V are the known parts of the island charge and voltage matrices, respectively. The work done by the voltage sources is given by:

$$W = \sum_n \int V_n(t) i_n(t) dt, \tag{5}$$

where $V_n(t)$ is the voltage of the nth voltage source, and $i_n(t)$ is the current through the nth voltage source.

The tunnel rate, Γ, for a particular tunnel event is given by:

$$\Gamma = \frac{\Delta F}{e^2 R_T \left(1 - \exp\left(-\frac{\Delta F}{kT}\right)\right)}, \tag{6}$$

where ΔF is the change in free energy caused by this particular tunnel event, (index) R_T, is the tunnel resistance of the tunnel junction through which the electron is transported, and kT is the thermal energy (k is the Boltzmann's constant, and T is the temperature). Once the tunnel rates for all possible tunnel

events are known the actually occurring event is determined using a Monte Carlo method combined with an exponential distribution of tunnel events. The time duration of a particular tunnel event is given by:

$$\Delta t = -\frac{\ln(r)}{\Gamma}, \tag{7}$$

where r is an evenly distributed random number in the interval [0, 1]. Among all possible tunnel events, the event with the shortest time duration takes place.

Single-electron majority gate

Circuit of single-electron majority gate simulated using the SIMON simulator [8] Fig. 1. Also figured gate can be used as three input majority gate if we place logical «0» on one of inputs and logical «1» on another one:

$$Maj(x_1, x_2, x_3, 1, 0) = Maj(x_1, x_2, x_3). \tag{8}$$

Design of full-adder with 5-inputs majority gate

Majority gates with five or more inputs are beneficial in synthesis of complicated logic circuits, because these majority gates have wider functionalities.

However, increasing of inputs number to more than five in using of single-electron transistors leads to dramatic complication of majority gate input circuits, it leads to inaccurate result in consequents of input signals and resistance scattering.

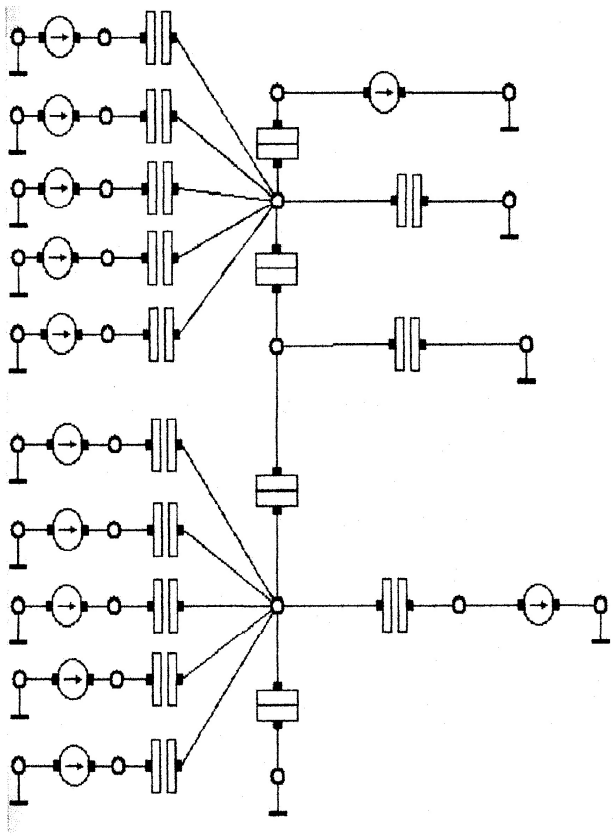

Fig. 1. Single-electron five-inputs majority gate circuit

Functionality of majority gate

The number of components of majority gate minimal equation with five inputs is equal to the number of combination 3 of 5 [8]:

$$\begin{aligned} Maj(x_1, x_2, x_3, x_4, x_5) &= x_1x_2x_3 + x_1x_2x_4 + x_1x_2x_5 + x_1x_3x_4 + x_1x_3x_5 \\ &+ x_1x_4x_5 + x_2x_3x_4 + x_2x_3x_5 + x_2x_4x_5 + x_3x_4x_5 = x_1\#x_2\#x_3\#x_4\#x_5. \end{aligned} \tag{9}$$

It is possible to do 128 different logic functions on one majority gates with 5 inputs and direct output and only 16 logic functions on majority gate with 3 inputs and direct output in the table.

It could be notice that the number majority functions $Maj(\overline{x_1}, \overline{x_2}, ..., \overline{x_n})$ is equal to 2^n (n is odd number).

The table shows that three inputs AND and OR gates are performed with majority gate and constant voltage levels on two inputs of gate:

$$\begin{aligned} Maj(\overline{x_1}, \overline{x_2}, \overline{x_3}, 0, 0) &= \overline{x_1}\,\overline{x_2}\,\overline{x_3}, \\ Maj(x_1, x_2, x_3, 1, 1) &= x_1 + x_2 + x_3. \end{aligned} \tag{10}$$

Synthesis of one-bit adder based on five inputs majority gate

It is possible to build the most rational circuit of one-bit adder with using of five inputs majority gates.

Indeed, it could be seen in the table that $x_4 = x_5 = \overline{C}$.

$$\begin{aligned} S = Maj(x_1, x_2, x_3, \overline{C}, \overline{C}) &= x_1\#x_2\#x_3\#\overline{C}\#\overline{C} \\ &= x_1\overline{C} + x_2\overline{C} + x_3\overline{C} + x_1x_2x_3 \\ &= \overline{C}(x_1 + x_2 + x_3) + x_1x_2x_3. \end{aligned} \tag{11}$$

This equation completely match with sum equation of one-bit adder.Structural circuit of one-bit adder which is built on one five inputs and one three inputs majority gates is shown in Fig. 2.

Functions of 5-inputs majority gate

Function arguments	Meaning of function in Boolean	Number of this type functions
x_1, x_2, x_3, x_4, x_5	$x_1x_2x_3 + x_1x_2x_4 + x_1x_2x_5 + x_1x_3x_4 + x_1x_3x_5 + x_2x_3x_4 + x_2x_3x_5 + x_2x_4x_5 + x_3x_4x_5 + x_1x_4x_5$	32
$x_1, x_2, x_3, x_4, 0$	$x_1x_2x_3 + x_1x_2x_4 + x_1x_3x_4 + x_2x_3x_4$	16
$x_1, x_2, x_3, x_4, 1$	$x_1x_2 + x_1x_3 + x_1x_4 + x_2x_3 + x_2x_4 + x_3x_4$	16
x_1, x_2, x_3, x_4, x_4	$x_1x_4 + x_2x_4 + x_3x_4 + x_1x_2x_3$	24
$x_1, x_2, x_3, x_3, 0$	$x_1x_3 + x_2x_3$	12
$x_1, x_2, x_3, x_3, 1$	$x_1x_2 + x_3$	12
$x_1, x_2, x_3, 0, 0$	$x_1x_2x_3$	8
$x_1, x_2, x_3, 1, 1$	$x_1 + x_2 + x_3$	8
x_1, x_2, x_3	$x_1x_2 + x_2x_3 + x_1x_3$	8
$x_1, x_2, 0$	x_1x_2	4
$x_1, x_2, 1$	$x_1 + x_2$	4

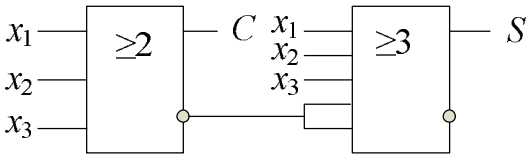

Fig. 2. Full-adder builted on majority gates

Results of full-adder simulation

In Fig. 3 shown time diagrams of Full adder simulation by SIMON [8].

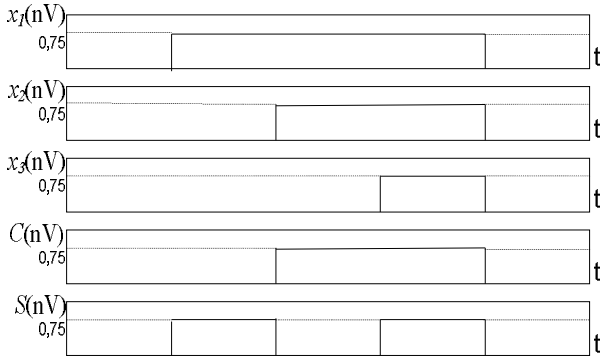

Fig. 3. Results of full-adder simulation

Conclusions. Current state of electronic technology development analysis has allowed to simulate single-electron adder with a minimum number of SET based nanoelements and nanocircuits.

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О. С. Мельник, В. О. Козаревич, В. В. Івахнюк. Автоматизоване проектування одноелектронних наносхем

Запропоновано наносхему на базі одноелектронних транзисторів з використанням пятивхідного мажортиарного елементу для комп'ютерного моделювання повного однорозрядного суматора.

Ключові слова: наноелектроніка; одноелектронні схеми; логічні елементи; мажоритарні елементи.

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А. С. Мельник, В. А. Козаревич, В. В. Ивахнюк. Автоматизированное проєктирование одноєлектронных наносхем

Предложено компьютерное проектирование наносхемы одноэлектронного одноразрядного сумматора на базе пятивходовых мажоритарных элементов.

Ключевые слова: наноэлектроника; одноэлектронные схемы; логические єлементы; мажоритарные єлементы.

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