UDC 004.94:621.389:53.086(045)

[1]O. S. Melnyk,
[2]A. V. Maksymenko,
[3]A. D. Sverdlova

COMPUTER SIMULATION OF SINGLE-ELECTRON LOGIC GATES

Institute of Air Navigation, National Aviation University, Kyiv, Ukraine
E-mails: [1]melnyk.ols@gmail.com, [2]maxisery@gmail.com, [3]miss.bookmark@yandex.ua

Abstract*—Nanoelectronic three-input element AND gate was examined. It is composed from 5 tunnel junctions, 3 capacitors and 4 voltage sources. The circuit, mentioned below, represent simple 3-input AND gate but with much lower energy consumption. However, it request specified conditions.*

Index Terms—nanoelectronics, quantum cellular automata, majority gate, single-electron circuits, logic gates.

I. INTRODUCTION

Microelectronic industry has gone through to the production of 100 nm structures to maintain the level of miniaturization that has stimulated the development until now. With decreasing size of integrated MOSFET devices limitations become more critical. The biggest problem is found in the task of electron tunneling through the thin oxide layer under gate. To simplify this process, new types of dielectrics are developed.

The most promising technologies in this field are quantum dots automates and single-electron devices. Single-electronics - a technology that allows you to control the transfer and positioning of one or a small number of electrons. Single-electron technology will allow creating ultrafast processors with low power consumption. The principle of this technology is based on the effect of the Coulomb blockade and tunneling [1]. After research of the effect this subject began to pay more attention as an opportunity to create higher integrated circuits with lower power consumption.

Several single-electron devices have been mentioned in the literature: single-electron memory, inverters, majority and logic elements [2]. With the growing need for computer modeling elements began to appear appropriate software.

This work presents three-input logic gate AND simulated with computer-aided design (CAD) system SIMON [3]. The method used for simulations is Monte-Carlo method. There were used five tunnel junctions, four quantum islands and three capacitors. Simulation of the device has been proven its efficiency, but there are a few refinements.

II. SINGLE-ELECTRON CIRCUITS

Single-electron circuits consist of connecting islands tunnel junctions, capacitors and voltage sources. To transfer an electron to the island, it should be given the energy higher than the Coulomb barrier [4], [5]:

$$E_c = \frac{e^2}{2C_i},$$

where C_i is island capacity, a e is electron charge. Single-electron nanocircuit contain islands which are connected in random order by tunnel junctions, capacitors and voltage sources (Fig. 1). Voltage sources have ideal settings, so their inner resistance equal to zero. Electrons tunnel regardless island to island. Resistance of tunnel junctions must be greater than the fundamental quantum impedance to localize an electron within the island, Ohm :

$$R = R_q = \frac{h}{e^2} \cong 25{,}813,$$

where h is Plank's constant.

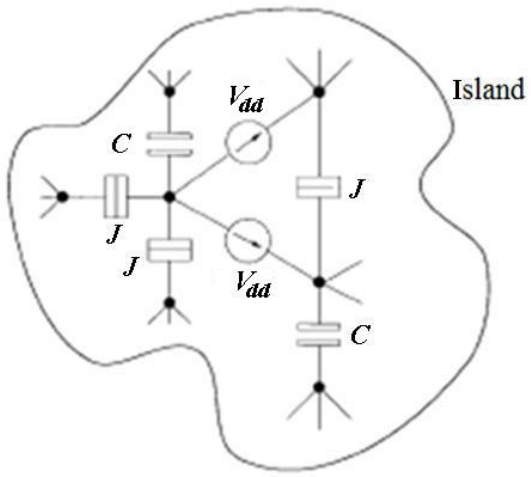


Fig. 1. Single-electron circle with tunnel junctions, capacitors and voltage sources

where J is tunnel junction; C is capacitor; V_{dd} is voltage source.

On the other hand, the fundamental equation describing electron tunneling between islands and, thus, nanocircuit takes different states. One of them is crucial. State is determined by voltage power supply and distribution of charges between Coulomb islands. Neglecting background charge, each island accumulates a certain number of elementary charges. However, in case the permanent voltage sources, its calculated infinite number of position. When it's required to calculate the fundamental equations shall consider a limited number of states. You will find out the probability of state as a result.

It's necessary to determine all the possible quantum transitions to simulate the tunnel junction. Tunneling probability depends on the free energy caused by the event. The free energy of one-electron scheme is the difference of electrostatic energy stored in the capacitor and the work performed by voltage sources:

$$F = U - W.$$

Electrostatic energy U can be determined:

$$U = \frac{1}{2}(q, v)\begin{pmatrix} V \\ Q \end{pmatrix},$$

where q and v are unknown matrixes of voltage and charge of islands, so V and Q are known matrixes respectively. In that case, work done by voltage sources:

$$W = \sum\nolimits_n \int V_n(t) i_n(t) dt,$$

where $V_n(t)$ and $i_n(t)$ are voltage and current pass through n source.

Tunneling probability, Γ, for certain tunnel junction:

$$\Gamma = \frac{\Delta F}{e^2 R_T \left[1 - \exp\left(-\frac{\Delta F}{kT}\right)\right]},$$

where ΔF is change of free energy caused by event; R_T is tunnel junction resistance; kT is thermodynamic energy. Resulting event will be determined, according Monte-Carlo method and exponential distribution, as soon as all probabilities will be known.

Duration of event can be determined:

$$\Delta t = -\frac{\ln(r)}{\Gamma},$$

where r is random number on interval [0,1]. According this, the shortest event will take place.

III. Single-electron three-input gate AND

Three-input logical element AND is showed on Fig. 2. The main island of $N1$–$N4$ interconnected with tunnel junctions $J1$–$J5$ and by capacitors $C1$–$C3$ with a logical vector.

Tunnel junctions and capacitors have such characteristics:

$C1$ – 0.4 aF, $C2$ – 0.6 aF, $C3$ – 0.8 aF,
$J1$ – 300 kOhm, 1.2 aF,
$J2$ – 300 kOhm, 1.15 aF,
$J3$ – 300 kOhm, 1.05 aF,
$J4$ – 100 kOhm, 0.9 aF,
$J5$ – 10 MOhm, 0.98 aF.

$J5$ has a higher resistance and capacitance so charge could accumulate and be detected. The voltage source V_{dd} is -0,115 V. The negative voltage value allows work with positive logic pulses.

Voltage sources $V1$, $V2$, $V3$ act as logic inputs and generates only 2 voltage levels: 0.1 V, which corresponds to a logical one; and -0.1 V, which corresponds to a logical zero. Logic charges are transferred through respective capacitors on the island of $N4$, where the charge is formed. The presence of a charge corresponding to a logical "1", and its absence – to a logical "0".

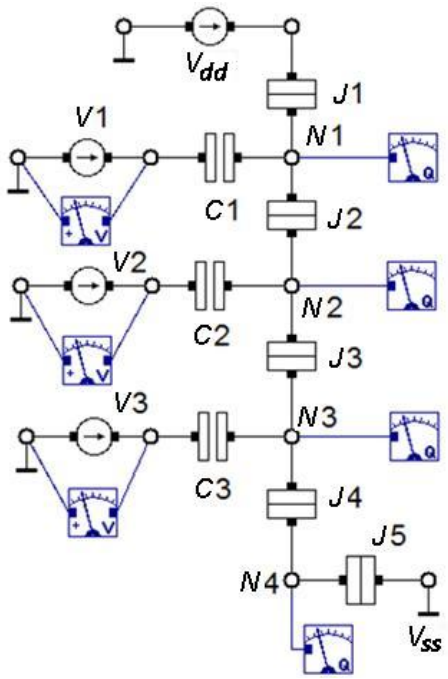


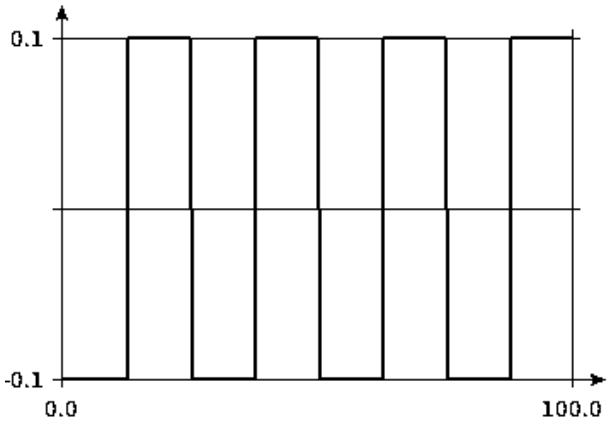
Fig. 2. Single-electron AND gate

IV. Result of simulation by CAD SIMON of three-input are AND

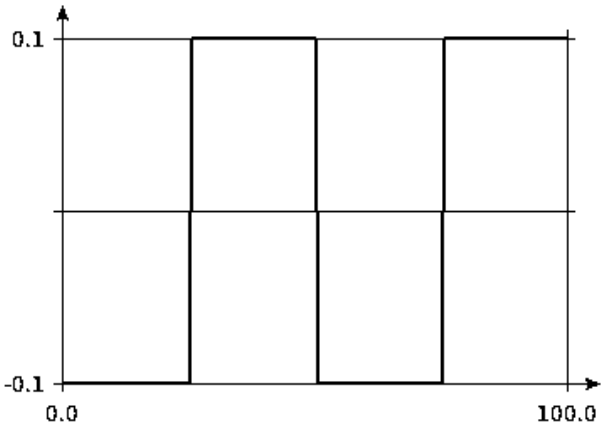
Logic sources $V1$, $V2$, $V3$ simulate logic pulses (Fig. 3,a,b,c). The charge on $QN4$ (Fig. 3,d) is positive only when the logical vector equal to [111]. That means all three sources of generating logic voltage 0.1 V. The transition between logic "1" and "0" and vice versa does not lead to system instability.

Changes voltage between "0" and "1" are almost idial. That's meen that time spant by logical voltage source is less than one nanosecond.

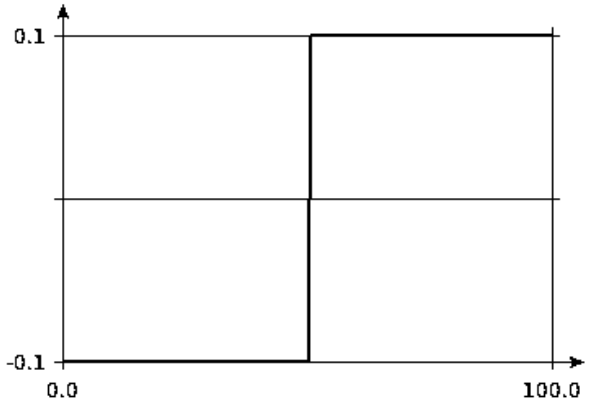
Still it have its trasitional period, but it don't cause any unexpected and unpredictable results.



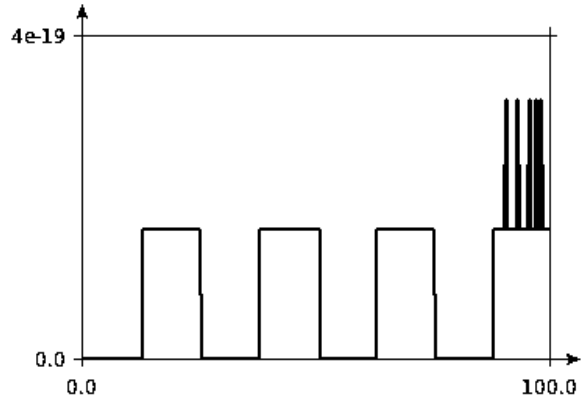
a



b



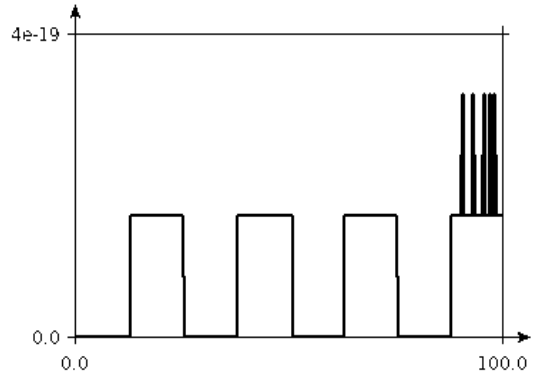
c



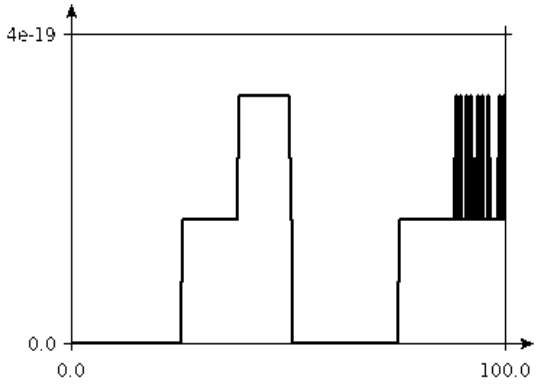
d

Fig. 3. Wawes-forms of three-inputs gate AND simulation

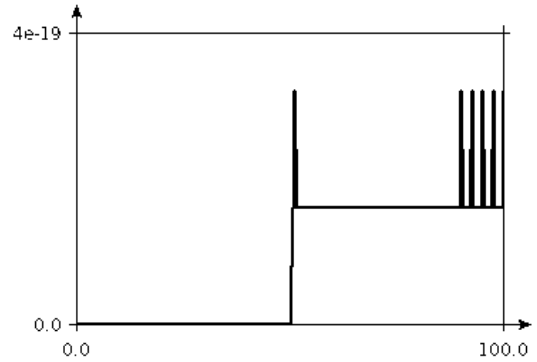
On Figure 4 it is displayed the results of collecting electrons in quantuum nodes n1(a), n2 (b), n3 (c) of electric logical scheme. These odd electrons cause gate switching correspondin to the results of modeling shown on a previous Fig. 3,d.



a



b



c

Fig. 4. Charges on intermediate islands *N*1–*N*3

V. CONCLUSIONS

In this article, the results of modeling single-electron three-input device. As a result, we received properly working unit, but with some assumptions. The final pulse on Fig. 3,d may be a uniform in a certain inertia measurement or use. However, it is not homogeneous in the general definition, but can be used, in the future, to operate with other devices, if necessary.

REFERENCES

[1] Ch. R. K. Marrian (Ed.). “Nanometer-sale science and technology.” *Proceedings of the IEEE* (special issue), no. 85, pp. 481–704. 1997.

[2] Compano, R.; Molenkamp, L.; Paul, D. J. 2000. “European Comission IST Programme.” *Future and Emerging Tecnologies, Technology Road-map For Nanoelectronics*.

[3] Wasshuber, C. “SIMON – A simulator for single-electron tunnel and circuit.” *IEEE Transactions on Computer-aided desing*, no. 16, 1999. pp. 937–944.

[4] Tsimperidis, I. “A single-electron three-input AND gate.” *Microelectronics Journal*, no. 33, 2002. pp. 191–195.

[5] Melnyk, O. S. “Computer-aided design of single-electron nanocircuits.” *Electronics and Control systems*, no. 3 (37). 2013. pp. 71–74.

Received 17 February 2014

Melnyk Oleksandr. Candidate of technical science. Associate Professor.
Electronic Department, National Aviation University, Kyiv, Ukraine.
Education: Kyiv Polytechnic Institute, Kyiv, Ukraine (1971).
Research area: Nanoelectronics, Computer-aided design of nanoelectronic circuits, Simulation of single-electron circuit.
Publications: 142.
E-mail: melnyk.ols@gmail.com

Maksymenko Artem. Bachelor.
Electronic Department, National Aviation University, Kyiv, Ukraine.
Education: National Aviation University, Kyiv, Ukraine (2014).
Research area: Simulation of single-electron circuit.
Publications: 3.
E-mail: maxisery@gmail.com

Sverdlova Anastasia. Bachelor.
Electronic Department, National Aviation University, Kyiv, Ukraine.
Education: National Aviation University, Kyiv, Ukraine (2014).
Research area: Simulation of single-electron circuit.
Publications: 3.
E-mail: miss.bookmark@yandex.ua

О. С. Мельник, А. В. Максименко, А. Д. Свердлова. Комп’ютерне моделювання одноелектронних логічних елементів

Розглянуто наноелектронний тривходовий елемент «І». Він складається з п’яти тунельних переходів, трьох конденсаторів та чотирьох джерел напруги. Схема представляє простий тривходовий елемент «І», але з набагато меншою енергією. Проте потребуються певні умови моделювання.

Ключові слова: наноелектроніка; квантовий клітинний автомат; мажоритарний елемент; одноелектронні схеми; логічні елементи.

Мельник Олександр Степанович. Кандидат технічних наук. Доцент.
Кафедра електроніки, Національний авіаційний університет, Київ, Україна.
Освіта: Київський політехнічний інститут, Київ, Україна (1971).
Напрям наукової діяльності: наноелектроніка, автоматизовані системи проектування, симулювання одноелектронних схем.
Кількість публікацій: 142.
E-mail: melnyk.ols@gmail.com

Максименко Артем Володимирович. Бакалавр.
Кафедра електроніки, Національний авіаційний університет, Київ, Україна.
Освіта: Національний авіаційний університет, Київ, Україна (2014).
Напрям наукової діяльності: моделювання одноелектронних схем.
Кількість публікацій: 3.
E-mail: maxisery@gmail.com

Свердлова Анастасія Дмитрівна. Бакалавр.
Кафедра електроніки, Національний авіаційний університет, Київ, Україна.
Освіта: Національний авіаційний університет, Київ, Україна (2014).
Напрям наукової діяльності: моделювання одноелектронних схем.
Кількість публікацій: 3.
E-mail: miss.bookmark@yandex.ua

А. С. Мельник, А. В. Максименко, А. Д. Свердлова. Компьютерное моделирование одноэлектронных логических элементов

Рассмотрен наноэлектронный трехвходовой элемент «И». Он состоит из пяти туннельных переходов, трех конденсаторов и четырех источников напряжения. Схема представляет простой трехвходовой элемент «И», но с гораздо меньшей энергией. Однако требуются определенные условия моделирования.
Ключевые слова: наноэлектроника; квантовый клеточный автомат; мажоритарный елемент; одноэлектронные схемы; логические элементы.

Мельник Александр Степанович. Кандидат технических наук. Доцент.
Кафедра электроники, Национальный авиационный университет, Киев, Украина.
Образование: Киевский политехнический институт, Киев, Украина (1971).
Направление научной деятельности: наноэлектроника, автоматизированные системы проектирования, симулирование одноэлектронных схем.
Количество публикаций: 142.
E-mail: melnyk.ols@gmail.com

Максименко Артем Владимирович. Бакалавр.
Кафедра электроники, Национальный авиационный университет, Киев, Украина.
Образование: Национальный авиационный университет, Киев, Украина (2014).
Направление научной деятельности: моделирование одноэлектронных схем.
Количество публикаций: 3.
E-mail: maxisery@gmail.com

Свердлова Анастасия Дмитриевна. Бакалавр.
Кафедра электроники, Национальный авиационный университет, Киев, Украина.
Образование: Национальный авиационный университет, Киев, Украина (2014).
Направление научной деятельности: моделирование одноэлектронных схем.
Количество публикаций: 3.
E-mail: miss.bookmark@yandex.ua