JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **7** No 1, 01004(4pp) (2015)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **7** № 1, 01004(4cc) (2015)

Analysis of Voltage Transfer Characteristics of Nano-scale SOI CMOS Inverter with Variable Channel Length and Doping Concentration

A. Daniyel Raj, C. Rajarajachozhan, Sanjoy Deb*

Dept. of ECE, BIT Sathy, Sathyamangalam, Tamilnadu-638401, India

(Received 08 November 2014; published online 25 March 2015)

During many decades, continuous device performance improvement has been made possible only through device scaling. But presently, due to aggressive scaling at the sub-micron or nanometer region, the conventional planner silicon technology is suffering from the fundamental physical limits. Such imposed limits on further downscaling of silicon planner technology have lead to alternative device technology like Silicon-On-Insulator (SOI) technology. Due-to some of its inherent advantages, the Silicon-On-Insulator (SOI) technology has reduced the Short-channel-effects (SCEs) and thus increased transistor scalability. Till now, intense research interests have been paid in practical fabrication and theoretical modeling of SOI MOSFETs but a little attention has been paid to understand the circuit level performance improvement with nano-scale SOI MOSFETs. The circuit level performance analysis of SOI MOSFET is highly essential to understand the impact of SOI technology on next level VLSI circuit and chip design and for doing so device compact models are high on demand. In such scenario, under present research, a physics based compact device model of SOI MOSFET has been developed. At the first phase of the compact model development, a physics based threshold voltage model has been developed by solving 2-D Poisson's equation at the channel region and at the second phase, a current-voltage model has been developed with drift-diffusion analysis. Different SCEs, valid at nano-scale, are effectively incorporated in threshold voltage and Current-Voltage model. At the third phase, using the compact model, the Voltage Transfer Characteristics (VTC) for a nano-scale SOI CMOS inverter has been derived with graphical analysis. The impacts of different device parameters e.g.; channel length and channel doping concentration on VTC has been investigated through simulation and the results have been analyzed.

Keywords: MOSFET, SOI, CMOS Inverter, Voltage transfer characteristics.

PACS numbers: 85.30.Tv, 85.35. – p

1. INTRODUCTION

Under present electronics era, the CMOS technology is widely used for circuit design for numerous applications [1]. Till now performance improvement of CMOS technology has been achieved by increasing the speed and decreasing, both the power consumption and size of its two fundamental building blocks, one nmos and one pmos device [2]. In recent time, as the scaling of planar MOS is facing significant challenges, several nonconventional geometry MOS based CMOS structures have been studied experimentally as well as theoretically [2]. Among the nonconventional MOS structures, Silicon-On-Insulator (SOI) technology has received much attention of the researchers due to some of its inherent functional advantages [3]. The SOI CMOS technology offers many advantages over bulk CMOS technology, in particular, higher speed, high radiation tolerance, lower parasitic capacitance, lower short channel effects, better current deliverability, manufacturing compatibility with the existing CMOS technology [4]. Intense research on experimental fabrication and theoretical modeling of SOI MOSFET has been carried out during last decades but till now, little attention has been paid to understand its circuit level performance improvement compared to conventional MOSFET [5]. But to understand the true impact of SOI technology in next generation CMOS VLSI, the SOI MOSFET based circuit design and its performance analysis are truly essential. In such context, the development of SPICE compatible fast converging, accurate SOI compact models and designing some circuits using those, are highly essential [6].

In the present research work, a simple but accurate compact model of nano-scale SOI MOSFET has been derived. At the first phase of the compact model development, 2D Poisson's equation has been solved at the channel region and from that a threshold voltage expression has been derived for SOI MOSFET. Different SCEs like drain induced barrier lowering (DIBL) or 2D charge sharing (2DCS) are incorporated in analytical threshold voltage model. At the next phase, the threshold voltage model has been incorporated into drift-diffusion analysis to develop a current-voltage model. At the final phase, using Current-Voltage characteristics of nmos and pmos, the Voltage Transfer Characteristics (VTC) of a SOI CMOS inverter has been derived using graphical approach. Lastly, the effect of deferent device parameters on VTC are theoretically studied and analyzed.

2. ANALYTICAL MODELING

For short channel device, the potential profile in the channel is two-dimensional in nature [7]. Threshold voltage can be calculated by solving 2-D Poisson's equation in the channel and current-voltage model can be formed from simple drift-diffusion analysis [8-9]. A layered structure of SOI MOSFET for compact model formulation is shown in Fig. 1. Let t_{gox}, t_{Si}, t_{box}, t_{sub} and L be the thicknesses of gate oxide, silicon channel layer, buried layer layer, substrate layer and metallurgical channel length of the device, respectively.

* sanjoydeb@bitsathy.ac.in

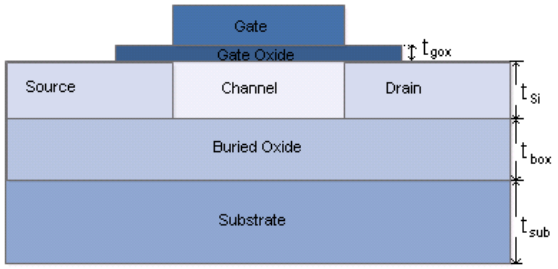

Fig. 1 – A SOI MOSFET layered structure

2.1 Threshold Voltage Modeling

The 2-D Poisson's equation in the two-dimensional channel region of the depleted silicon film body ($0 \le x \le L$, $0 \le y \le t_{si}$) can be written as [10];

$$\frac{\partial^2 \alpha(x,y)}{\partial x^2} + \frac{\partial^2 \alpha(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}, \tag{1}$$

where, $\alpha(x, y)$ is the 2-D potential profile in the silicon channel, N_A is the doping concentration of the p-type channel and the substrate and ε_{Si} is the permittivity of silicon. Considering a second order potential approximation, the 2D potential profile in the channel is written as [11];

$$\alpha(x,y) = F_1(x) + F_2(x)y + F_3(x)y^2 \tag{2}$$

At the front and back channel interfaces, uniform electric field are considered and the surface potentials are abbreviated as $\alpha_{sf}(x)$ and $\alpha_{sb}(x)$, respectively. The four boundary conditions are given as [10-11];

1. Electric flux at the gate / front-oxide interface is continuous so at $y = 0$;

$$\frac{\partial \alpha(x,y)}{\partial y} = -E_{sf}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_{gs}^{'} - \alpha_{sf}(x)}{t_f} \tag{3}$$

2. Electric flux at the interface of buried oxide and the back-channel is continuous so at $y = t_{Si}$

$$\frac{\partial \alpha(x,y)}{\partial y} = -E_{sb}(x) = -\frac{\varepsilon_{box}}{\varepsilon_{Si}} \frac{V_{ss}^{'} - \alpha_{sb}(x)}{t_{box}} \tag{4}$$

3. The potential at the source end is ($L = 0$);

$$\psi(x = 0, y = 0) = V_{bi} \tag{5}$$

Where, V_{bi} is the built in potential in the channel.

4. The potential at the drain end is ($L = L$);

$$\psi(x = L, y = 0) = V_{bi} + V_{DS} \tag{6}$$

Where, ε_{BL} is the dielectric permittivity of silicon dioxide, V'_{gs} and V'_{ss} are the effective applied front and back channel voltages. The front and back channel voltages are expressed as $V'_{gs} = V_{gs} - V_{ffb}$ and $V'_{ss} = V_{ss} - V_{bfb}$, where V_{ffb} and V_{bfb} are the front and back channel flat band voltages, respectively. The values of the coefficients $F_1(x)$, $F_2(x)$ *and* $F_3(x)$ derived by solving equations 2 and 3, 4 and device long channel threshold voltage can be obtained as [10-11];

$$V_{th}^{long} = V_{ffb} + \left(\frac{C_f}{C_{box}} + \frac{C_f}{C_{Si}}\right)^{-1} \left[\begin{array}{l} \left(1 + \frac{C_f}{C_{box}} + \frac{C_{gox}}{C_{Si}}\right)(2\varphi_F) \\ -V_{ss}^{'} + \frac{qN_A t_{Si}\left(1 + 2\frac{C_{Si}}{C_{box}}\right)}{2C_{Si}} \end{array}\right] \tag{7}$$

where, $2\varphi_F = \frac{K_B T}{q} \ln\left(\frac{N_A}{N_i}\right)$ is the Fermi potential in the silicon film. To encounter the lateral field in the channel the boundary conditions at source and drain side (eqn. 5, 6) have been incorporated and the final short channel threshold voltage is obtained as;

$$V_{th}^{short} = V_{th}^{long} + \frac{1}{\frac{\varepsilon_{Si}}{t_{Si}} r_4} [2\varphi_F - r_1 - 2\varphi_F r_3 - r_2 V_{ds}] \tag{8}$$

$$r_1 = \frac{V_{bi}[\sinh(\frac{L - x_{\min}}{\lambda}) + \sinh(\frac{x_{\min}}{\lambda})]}{\sinh(\frac{L}{\lambda})}$$

where

$$\text{and} \quad r_2 = \frac{\sinh(\frac{x_{\min}}{\lambda})}{\sinh(\frac{L}{\lambda})}$$

$$r_3 = 1 - \frac{[\sinh(\frac{L - x_{\min}}{\lambda}) + \sinh(\frac{x_{\min}}{\lambda})]}{\sinh(\frac{L}{\lambda})} \quad \text{and}$$

$$r_4 = \frac{[\frac{C_{gox}}{C_{box}} + \frac{C_{gox}}{C_{Si}}]}{[1 + \frac{C_f}{C_{box}} + \frac{C_f}{C_{Si}}]}.$$

Equation 8 can be further simplified as;

$$V_{th}^{short} = V_{th}^{long} + r_5 - r_6 V_{ds}$$

$$\text{where} \quad r_5 = \frac{2\varphi_F - r_1 - 2\varphi_F r_3}{\frac{\varepsilon_{Si}}{t_{Si}} r_4} \quad \text{and} \quad r_6 = \frac{r_2 t_{Si}}{\varepsilon_{Si} r_4} \tag{9}$$

2.2 Current Voltage Modeling

Incorporating the threshold voltage into drift-diffusion analysis, I-V expression at cut-off, linear and saturation region for nmos has been derived as [12];

$$I_{ds,n} = 0 \quad \text{for} \quad V_{gs} < V_{th,n}^{short} \tag{10}$$

$$I_{ds,n} = \frac{W_n}{L_n} \mu_n C_{gox} V_{ds}\left(1 + \lambda_n V_{ds}\right) \left(\begin{array}{l} V_{ds} - V_{th}^{long} \\ +r_5 - (r_6 + 0.5)V_{ds} \end{array}\right) \tag{11}$$

$$\text{for} \quad V_{gs} > V_{th,n}^{short} \text{ and } \quad V_{ds} < \left(V_{gs} - V_{th,n}^{short}\right)$$

$$I_{ds,n} = \frac{W_n}{L_n}\mu_n C_{gox} V_{ds}\left(1+\lambda_n V_{ds}\right)$$
$$\left(\left(1-r_6\right)V_{ds} - V_{th}^{long} + r_5\right)^2 \qquad (12)$$
for
$$V_{gs} > V_{th,n}^{short} \; and \quad V_{ds} \geq \left(V_{gs} - V_{th,n}^{short}\right)$$

Where $V_{th,n}{}^{short}$ is the threshold voltage, μ_n is the mobility of the electron, L is the channel length, W is the channel width and λ_n is the channel length modulation factor respectively for the nmos. Similarly considering N_D (n-type channel doping concentration) in place of N_A, μ_p in place of μ_n, W_p in place of W_n.

2.3 Voltage Transfer Characteristics

The voltage-transfer characteristic (VTC) can be graphically deduced by superimposing the current-voltage characteristics of the nmos and the pmos devices [13]. Such a graphical construction is traditionally called a load-line plot and it requires that the $I_{dn} - V_{ds}$ curves of the nmos and pmos devices are transformed onto a common coordinate set [13]. The input voltage V_{in}, the output voltage V_{out} and the nmos drain current I_{dn} as the variables of choice and the pmos $I_{dp} - V_{ds}$ relations has been translated into this variable space. The resulting load lines are plotted in Fig. 2.

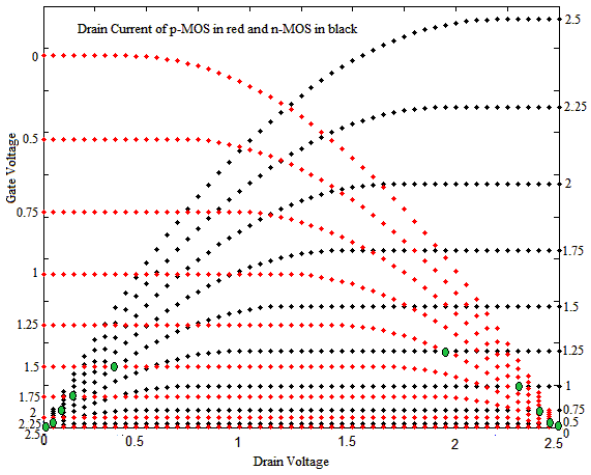

Fig. 2 – Superimposed I-V characteristics of n-MOS and p-MOS

For a DC operating points to be valid, the currents through the n-MOS and p-MOS devices must be equal and graphically this means that the dc points must be located at the intersection of corresponding load lines [13]. In Fig. 2, a number of those points (for V_{in} = 0, 0.5, 0.75, 1 and 1.25 V) are marked and all these observed points are translated into the VTC [13]. One of the important VTC parameter is switching threshold, (V_M) which is defined as the point where $V_{in} = V_{out}$. Its value can be obtained graphically from the intersection of the VTC with the line given by $V_{in} = V_{out}$.

3. RESULT AND DISCUSSIONS

The VTC of an inverter with higher noise margin will exhibit a very narrow high-to-low transition zone and V_M at the middle of maximum V_{out} or V_{in} [14]. Steeper transition from high-to-low sate or vise versa will signify high gain and better noise immunity [14].

Table 1 – Parameter values used for simulation

Parameter	Value
N_A	10^{21} m^{-3}
N_{SUB}	10^{21} m^{-3}
$N_{S\text{-}D}$	10^{26} m^{-3}
N_G	10^{26} m^{-3}
V_{SUB}	0 V
V_{DS}	1 V
T	300 K
t_{gox}	3 nm
t_{Si}	5 nm
t_{box}	50 nm
V_{sat}	8.3×10^4 mS^{-1}
$\mu_{0,n}$	0.0612 m^{2}V^{-1}S
$\mu_{0,p}$	0.0300 m^{2}V^{-1}S
W_n	1 μm
W_p	2 μm

For the present analysis, results are simulated using the parameter values (default values) given in the Table 1 and any other specific change in parameter values from the default values are mentioned at the figure caption.

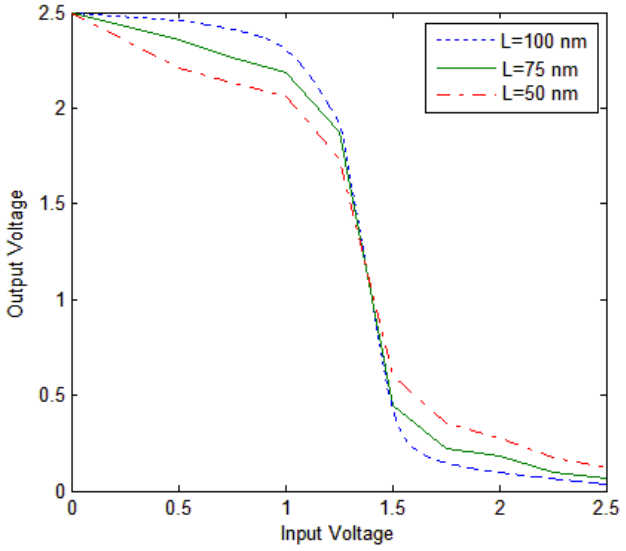

Fig. 3 – Variation of VTC with different channel lengths for $N_A = N_D = 10^{21}$/m^3

Under present analysis it has been found slope of VTC is steeper for longer channel and with the channel length reduction the steepness of VTC reduces (Fig. 3). The value of V_M for L = 100, 75 and 50 nm have been found 1.46, 1.35 and 1.29 volts, respectively which signify higher noise margin with longer channel length. This fact is attributed from the higher SCEs with short channel device compared to longer channel device [15].

Fig. 4, shows the variation of VTC with variable channel doping concentration, when channel length has been kept constant at 100nm. The switching threshold value for $N_A = N_D = 10^{19}$, 10^{20} and 10^{21}/m^3 have been found 1.45, 1.30 and 1.23 volts, respectively. Short channel effects like two-dimensional charge sharing is

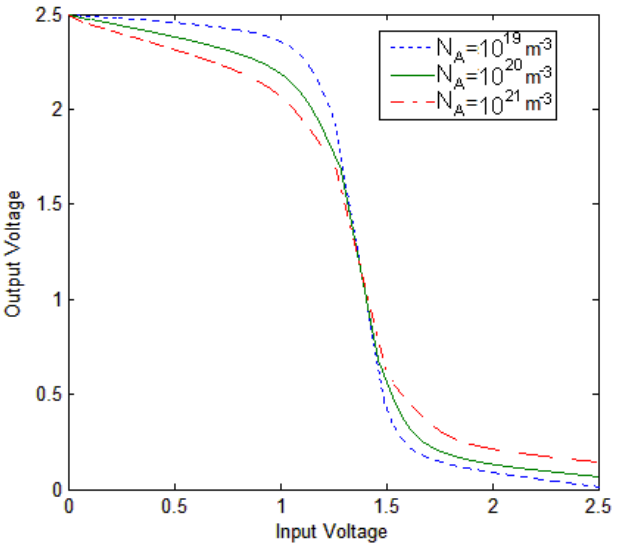

Fig. 4 – Variation of VTC with N_A (= N_D) for channel length 100 nm

much more pronounced with lower channel doping concentration and thus makes VTC flatter with reduced channel doping concentration [15].

4. CONCLUSION

In the present analysis, a simple but accurate compact threshold voltage model has been developed for nano-scale SOI MOSFET by solving 2D Poisson's equation at the channel region. Different SCEs are incorporated in analytical threshold voltage model and finally threshold analysis has been extended into Current-Voltage model for nmos and pmos. Using that compact approach, the VTC of a nano-scale SOI CMOS inverter has been derived using graphical analysis. The impact of different device parameters on VTC has been analyzed through simulation. It has been found that although scaling down the channel length has given advantage in terms of area but it has reduced the noise margin as device with shorter channel length is less immune to different SCEs. Reduction of channel doping concentration will also induce more noise effect as reflected with flatter VTC slop with lower doping concentration. So, the SOI CMOS circuit's efficiency can be significantly improved with successful reduction of SCEs at nano-scale and that can be achieved through new device structures and material property improvement.

REFERENCES

1. Yong-Bin Kim, *T. Electr. Electron. Mater.* **10** No 1, 21 (2009).
2. Y. Taur, *IBM J. Res. Dev.* **46**, 213 (2002).
3. Wang Runsheng, Yu Tao, Huang Ru, Wang Yangyuan, *Sci. China Inf. Sci.* **56**, 062403 (2013).
4. Qian Xie, Chia-Jung Lee, Jun Xu, C. Wann, J.Y.-C. Sun, Yuan Taur, *IEEE T. Electron Dev.* **60** No 6, 1814 (2013).
5. The International Technology Roadmap for Semiconductor (ITRS), Emerging Research Devices, (2011).
6. A.B. Bhattacharyya, *Compact MOSFET Models for VLSI Design* (Wiley-IEEE Press: 2009).
7. A. Majumdar, Z. Ren, S.J. Koester, W. Haensch, *IEEE T. Electron Dev.* **56** No 10, 2270 (2009).
8. K. Suzuki, S. Pidin, *IEEE T. Electron Dev.* **50** No 5, 1297 (2003).
9. G. Zhang, Z. Shao, K. Zhou, *IEEE T. Electron Dev.* **55** No 3, 803 (2008).
10. Sanjoy Deb, et al., *IEEE T. Nanotechnol.* **11** No 3, 472 (2012).
11. Sanjoy Deb, et al., *J. Semiconductor* **32** No 10, 104001 (2011).
12. Sanjoy Deb, et. al., *Int. J. Electron.* **98** No 11, 1465 (2011).
13. H. Neil, E. Weste, David M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Ed.* (Boston: Pearson/Addison-Wesley: 2010).
14. R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation, Third Ed.*, 1120 (Wiley-IEEE: 2010).
15. Sanjoy Deb, et al., *J. Nanoeng. Nanomanufacturing* **1** No 2, 177 (2011).