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Channel Length Effect on Subthreshold Characteristics of Junctionless Trial Material Cylindrical Surrounding-Gate MOSFETs with High-k Gate Dielectrics

Fairouz Lagraf[*,1,2], Djamil Rechem[3,4], Kamel Guergouri[1,2], Mourad Zaabat[1,2]

[1] *Laboratory of Active Components and Materials, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[2] *Faculty of Exact Sciences, Natural and Life Science, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[3] *Laboratory of Materials and Structure of Electromechanical Systems and their Reliability, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[4] *Department of Electrical Engineering, Faculty of Sciences and Applied Sciences, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*

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The intensive decrease of channel length for a MOS transistor imposes extensive constraints notably for controlling the short channel effects (SCEs) in nanoscale MOSFET. These constraints can degrade the device performance, hence determining the limits of miniaturization of MOSFET in nanoelectronics applications. In order to reduce the degree of SCEs, a number of new architectures have been reported. Due to their higher scaling capabilities, the double-gate (DG) MOSFETs are expected to be maintained in future nanoelectronics applications. However, with the continuous miniaturization other serious challenges related to the maximum power dissipation and the fabrication cost still persist owing to the high cost techniques used for the elaboration of the *p-n* junctions. Recently, a new design called junctionless MOSFET without source/drain junctions has been proposed to be an excellent alternative to the conventional MOSFET. The major advantage of this structure resides on the enhanced fabrication procedure through the elimination of the *p-n* junctions. In this work, the impact of channel length and high-k gate dielectrics materials on the subthreshold characteristics of junctionless trial material cylindrical surrounding-gate MOSFETs (JLTMCSG-MOSFETs) with high-k gate dielectrics and trial material (TM) structure has been studied using two-dimensional analytical model. This model is based on the solution of Poisson's equation in continuous cylindrical regions using superposition method, where the Fourier-Bessel series and separation method have been used to obtain the accurate solution. The performance of low power JLTMCSG-MOSFETs is investigated in terms of surface potential distribution, electrical field, subthreshold current, drain induced barrier lowering (DIBL), subthreshold slope (SS) and threshold voltage (Vth). This study is carried out over a wide range of channel lengths and using high-k gate dielectrics. This study confirms that the analytical model used is useful not only for circuit simulations, but also for device design and optimization for both logic and analog RF circuits applications.

Keywords: Junctionless MOSFETs transistor, Channel length effect, High-k gate dielectrics, Nanoscale device modeling.

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1. INTRODUCTION

Since several decades ago, the size of the metal-oxide-semiconductor field-effect transistors (MOSFETs) did not cease to be miniaturized. The old MOSFET transistors used in the past were made of two *p-n* junctions with an effective channel length designed between them. MOSFET technology has reached its limits from the point of view of miniaturization, imposed by the gate tunneling current and the adverse short channel effects (SCEs) [1, 2]. This is why many new multiple gate structures such as double-gate (DG) [3], triple-gate (TG) [4], π-gate [5], Ω-gate [6], quadruple-gate (QG) and surrounding gate MOSFETs [7, 8] have become coveted research topics because of their high gate control ability and their high scaling [6]. Among these developed structures, the cylindrical surrounding-gate (CSG) MOSFET is considered as one of suitable candidates giving the possibility to reduce the SCEs for a specified oxide thickness and channel length [9, 10]. To overcome these challenges, junctionless (JL) transistors are suggested [11]. These transistors are known for their doping concentration, constant in the three regions; source, channel and drain, which allow junctionless technology with many advantages, for example, no abrupt junctions, difficult to control at the nanoscale, simpler manufacturing process and volume conduction. This is the probable cause of minimizing of the surface roughness scattering and flicker noise [12-15].

There are new structures proposed called Dual [16] and Trial [17] Material JLCSG-MOSFETs with different work function to improve carrier transport efficiency, which reduces the SCEs. In our previous work [18] we found that L1:L2:L3 = 1:2:3 is the best device structure of JLTMCSG-MOSFET to achieve high performance. It is for the first time to our knowledge that a trial material (TM) structure with a gate electrode and high-k gate dielectric was used to study the SCEs in JLTMCSG-MOSFETs. By the use of full two dimensional (2D) analytical model, the JLTMCSG-MOSFETs have been studied by solving the two dimensional Poisson's equation. Based on this model, surface potential, electrical field, subthreshold current, drain induced barrier lowering (DIBL), subthreshold slope (SS) and threshold voltage (Vth) have been investigated. Subthreshold current can be easily studied in both cases with and without high-k gate dielectrics permittivity.

* fairouzph@gmail.com

2. DEVICE STRUCTURE

The JLTMCSG-MOSFET consists of three gate materials $\phi_{M1} = 4.7e.\mathrm{V}$, $\phi_{M2} = 4.4e.V$, $\phi_{M3} = 4.4e.\mathrm{V}$, the channel region can be divided into three parts. Due to the cylindrical symmetry of the device structure, a cylindrical coordinate system, consisting on a radial direction (r) and a horizontal direction (z), was used. We use both SiO_2 and high-k dielectric TiO_2 (k = 80) as a high-k gate dielectric oxide [19, 20]. To avoid surface scattering because of the use of high-k dielectric as a gate oxide, SiO_2 is deposed near the silicon region with the SiO_2 thickness of t_{SiO2} = 1 nm and high-k dielectric thickness of 1 nm.

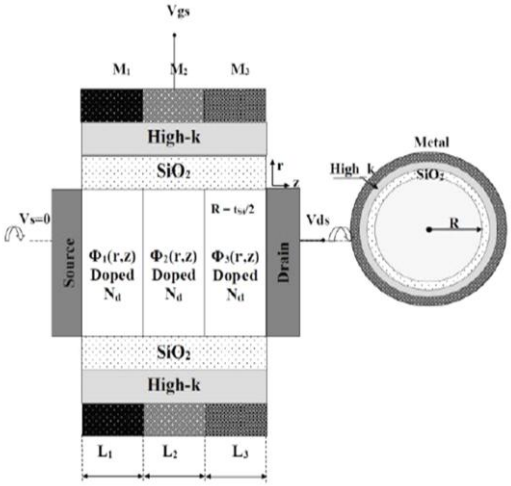

Fig. 1 – Cross-section view of JLTMCSG-MOSFETs

3. ANALYTICAL MODEL

3.1 Electrostatic Potential

By solving Poisson's equation in three regions of the channel, the electrostatic potential in JLTMCSG-MOSFET can be written as follows:

$$\frac{1\partial}{r\partial r}\left(r\frac{\partial}{\partial r}\Phi_i(r,z)\right)+\frac{\partial^2}{\partial z^2}\Phi_i(r,z)=\frac{qN_i}{\varepsilon_{Si}},\ i=1,2,3\,. \quad (1)$$

By the use of superposition technique, the electrostatic potential in each region of the channel can be written as [16]

$$\Phi_{\mathrm{i}}(\mathrm{r,z}) = \mathrm{V_i(r)} + \mathrm{U_i(r,z)}$$
$$\Phi_i(r,z) = V_i(r) + U_i(r,z),\ i=1,2,3, \quad (2)$$

where $V_i(r)$ and $U_i(r,z)$ are, respectively, the 1D solution obtained from the Poisson's equation and the 2D solution of the homogeneous Laplace equation obtained considering the boundary conditions [21]:

$$V_i(r)=\frac{qN_i}{4\varepsilon_{Si}}r^2+V_{gs}+\Phi_{MSi}-\frac{qN_i t_{ox}^{'}}{2\varepsilon_{ox}}-\frac{qN_iR^2}{4\varepsilon_{Si}}, \quad (3)$$
$$i=1,2,3,$$

where Φ_{MSi} represents the work function of different materials and is given by

$$\Phi_{Msi}=\Phi_{Mi}+\Phi_{Si},\ i=1,2,3, \quad (4)$$

where Φ_{Mi} is the metal work function and Φ_{Si} is the silicon work function.

Using the Fourier-Bessel series and separation method, the general solution $U_i(r,z)$ is expressed as [21]

$$U_i(r,z)=\sum_{n=1}^{\infty}\left[C_n^{(i)}\exp\frac{\alpha_n z}{R}+D_n^{(i)}\exp\frac{-\alpha_n z}{R}\right]J_0\left(\frac{\alpha_n}{R}\right), \quad (5)$$
$$i=1,2,3,$$

where α_n is the eigenvalue and satisfies the equation

$$\frac{\varepsilon_{ox}R}{t_{ox}^{'}\varepsilon_{Si}}J_0(\alpha_n)-J_1(\alpha_n)\alpha_n=0, \quad (6)$$

$J_i(x)$ is the first term Bessel function of the i-th order. The Fourier-Bessel series coefficients $C_n^{(i)}$ and $D_n^{(i)}$ are obtained by the boundary conditions.

3.2 Subthreshold Current Calculation

The current density (both drift and diffusion) can then be written as [21, 22]

$$J(r,z)=-q\mu_n n(r,z)\frac{d\Phi_n(z)}{dz}, \quad (7)$$

where $n(r,z)$ is the carrier concentration and μ_n is the electron mobility.

By integrating the current density $J(r,z)$ twice and through the z direction, we obtain

$$I_{ds}(z)=q\mu_n\frac{d\Phi_n(z)}{dz}\times$$
$$\times 2\pi\int_0^R rN_D\exp\left\{q\left[\Phi(r,\mathrm{z})-\Phi_n(z)\right]\Big/KT\right\}dr, \quad (8)$$

3.3 Threshold Voltage V_{th}

The threshold voltage is defined as the gate voltage which produces a minimum surface potential equal to twice the Fermi potential, i.e.,

$$\Phi_1(r=R,\mathrm{Z}=Z_{\min})=2\sqrt{C_1^{(1)}D_1^{(1)}}J_0(\alpha_1)+$$
$$+V_{gs}-\Phi_{MS}-\frac{qN_2t_{ox}^{'}R}{2\varepsilon_{ox}}, \quad (9)$$

$$\Phi_1(r=R,\mathrm{Z}=Z_{\min})=2\Phi_F,\ V_{gs}=V_{th}, \quad (10)$$

where

$$Z_{\min}=\frac{R}{2\alpha_1}\ln\frac{D_n^{(1)}}{C_n^{(1)}}, \quad (11)$$

$Z_{\min}$ is the minimum surface potential in region 1.

The threshold voltage can be obtained as

$$V_{th}=\Phi_{MS1}-U_t-\frac{(qN_1R)}{2C_{ox}}-\frac{\left(qN_1R^2\right)}{4\varepsilon_{Si}}-2\sqrt{Cn_1^1Dn_1^1}, \quad (12)$$

where

$$U_t = \frac{K_B T}{q} \tag{13}$$

4. RESULTS

Fig. 2 shows the surface potential with and without high-k gate dielectric as a function of channel position along the z direction. It can be noticed from the figure that the surface electrostatic potential in the channel region near the source is slightly higher when using high-k permittivity as a gate dielectric. This means that the injection of carriers from the source to the channel is more efficient, therefore the use of high-k gate dielectric improves the operation speed of the device.

The central horizontal electric field distribution for JLTMCSG-MOSFETs is shown in Fig. 3. It is found that there is an electric field peak in the middle of the channel of the JLTMCSG-MOSFETs that ensures a better average electric field across the channel. Therefore, the carrier transport efficiency and device speed increase.

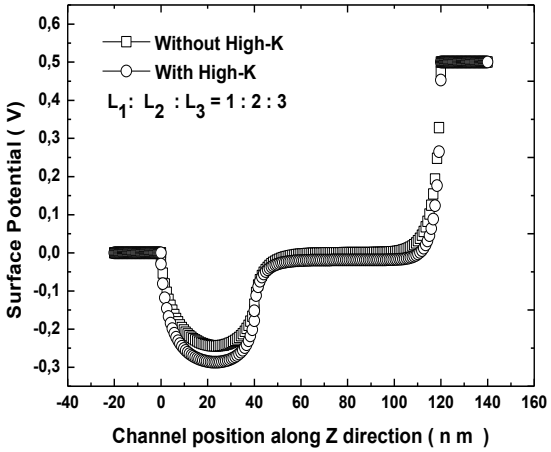

Fig. 2 – Surface potential profile for JLTMCSG-MOSFET with various ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are L = 120 nm, R = 10 nm, t_{ox} = 1 nm, V_{gs} = 0.2 V and V_{ds} = 0.5 V

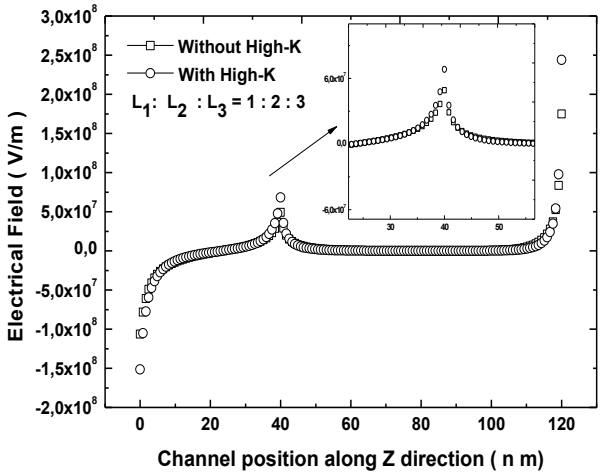

Fig. 3 – Electric field versus channel distance of JLTMCSG-MOSFET with various ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are L = 120 nm, R = 10 nm, t_{ox} = 1 nm, V_{gs} = 0.2 V and V_{ds} = 0.5V

A higher electric field is obtained with the high-k gate dielectrics.

Fig. 4 shows the subthreshold current of transfer characteristics of JLTMCSG-MOSFETs with and without high-k gate dielectric for the three different work functions of gate materials. It can be seen from this figure that the values of subthreshold current obtained using high-k gate dielectrics are lower than those obtained with SiO_2.

DIBL is a SCE in JLTMCSG-MOSFETs attributed to a reduction of the threshold voltage of the device under high drain bias. In JLTMCSG-MOSFETs, the DIBL effect is still a primitive problem and opened for further study, it is deduced using the following equation [19, 23]:

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \frac{V_{th1} - V_{th2}}{V_{ds1} - V_{ds2}}, \tag{14}$$

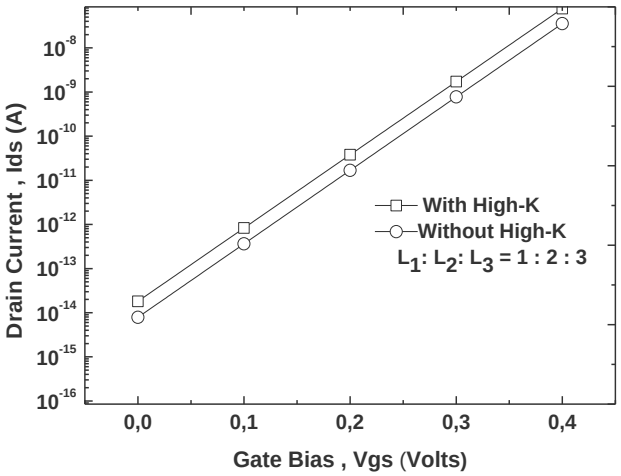

Fig. 4 – Subthreshold current versus gate voltage for JLTMCSG-MOSFETs with various silicon ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are the following: L = 120 nm, R = 10 nm, t_{ox} = 1 nm and V_{ds} = 0.5 V

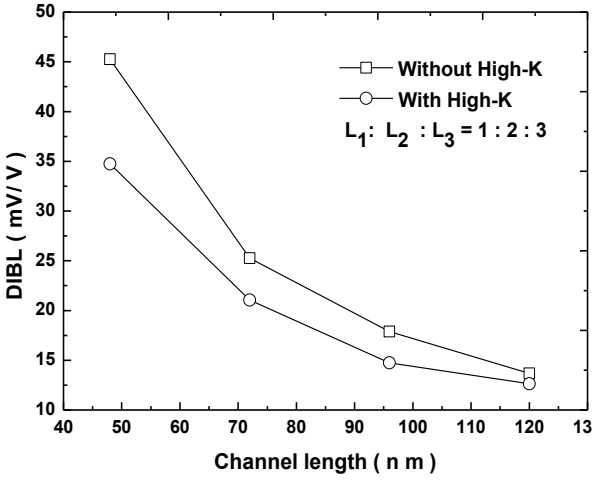

Fig. 5 – Drain induced barrier lowering with channel length for various ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are R = 10 nm, t_{ox} = 1 nm and $V_{ds\ low}$ = 0.05 V, $V_{ds\ high}$ = 1 V

In Fig. 5, the effect of different channel lengths on drain-induced barrier lowering (DIBL) with and with-

out a high-k dielectric gate is examined. We note that the DIBL decreases substantially with increasing channel length. We have a reduction of around 92 % of DIBL when L_g varies from 48 to 120 nm. It can be seen from this figure that the use of high-k gate dielectrics give an important reduction of DIBL.

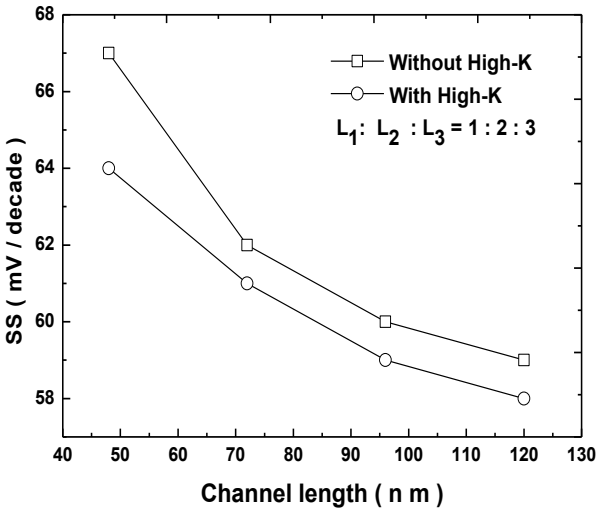

Fig. 6 - Subthreshold slope with channel length for various ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are R = 10 nm, t_{ox} = 1 nm and $V_{ds\ low}$ = 0.05 V, $V_{ds\ high}$ = 1 V

The subthreshold slope (SS) is defined as the gate voltage variation needed for the change of one decade in the drain current [23] given by

$$SS = \Delta V_{gs} / \Delta(\log I_{ds}). \quad (15)$$

A theoretical SS is around 60 mV/decade at room temperature [24] that is desired for low-threshold voltage and low-power operation of FETs scaled down to small size.

Fig. 6 shows the subthreshold slope for JLTMCSG-MOSFETs with and without high-k gate dielectric for different channel lengths. We observed a decrease in SS when channel length increases. Moreover, it is observed that the use of high-k gate dielectric significantly reduces the SS for the channel lengths in sub 120 nm regime.

The variation of threshold voltage against channel length is presented in Fig. 7 with and without high-k gate dielectric. From this figure, we can observe easily the effect of introducing high-k material as a gate

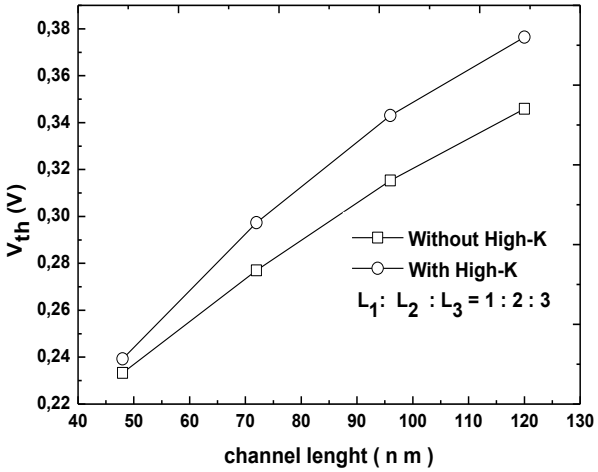

Fig. 7 – Subthreshold voltage with channel length for various ratios of L_1:L_2:L_3 = 1:2:3. The simulated device parameters are R = 10 nm, t_{ox} = 1 nm, V_{gs} = 0.3 V and V_{ds} = 0.5 V

dielectric on threshold voltage. Therefore, JLTMCSG-MOSFETs with high-k gate dielectric has a superior threshold voltage even channel length varies from 48 to 120 nm. Thus, the engineering of gate oxide is an important factor to improve device performances.

5. CONCLUSIONS

The impact of the channel length of nanoscale JLTMCSG-MOSFETs with high gate dielectric permittivity has been studied by the use of an analytical model based on the solution of two dimensional Poisson's equation.

A low subthreshold current when using high-k gate dielectric compared to the subthreshold current obtained with SiO_2 oxide has been observed. Also, we can see that the DIBL decreases substantially with increasing channel length, a better reduction can be obtained for a device with the high-k gate oxide. In addition, the results elucidate the influence of channel length and high-k gate oxide on SS and Vth. Better reduction of SCEs and an improvement in the device reliability have been also observed.

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Ефект впливу довжини каналу на порогові характеристики безперехідних циліндричних польових транзисторів із затвором з діелектриків з високою проникністю

Fairouz Lagraf[1,2], Djamil Rechem[3,4], Kamel Guergouri[1,2], Mourad Zaabat[1,2]

[1] *Laboratory of Active Components and Materials, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[2] *Faculty of Exact Sciences, Natural and Life Science, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[3] *Laboratory of Materials and Structure of Electromechanical Systems and their Reliability, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*
[4] *Department of Electrical Engineering, Faculty of Sciences and Applied Sciences, University Larbi Ben M'hidi Oum El Bouaghi, 4000, Algeria*

Інтенсивне зменшення довжини каналу для польового транзистора з контактом метал-напівпровідник у якості затвору (MOSFET) накладає значні обмеження, зокрема, на управління ефектами короткого каналу в нанорозмірних MOSFET. Ці обмеження можуть погіршити продуктивність пристрою, що визначає межі мініатюризації MOSFET в наноелектронних приладах. Для того щоб зменшити вплив ефектів короткого каналу, було повідомлено про ряд нових конфігурацій. Завдяки більш високим можливостям масштабування, в майбутньому очікуються польові транзистори з двома затворами (DG-MOSFET). Однак, при постійній мініатюризації інші серйозні проблеми, пов'язані з максимальною дисипацією потужності та вартістю виготовлення, все ще зберігаються внаслідок високих витрат, які використовуються для розробки *p-n*-переходів. Нещодавно була запропонована нова конструкція під назвою безперехідний MOSFET без переходів джерело/сток, що є відмінною альтернативою звичайним MOSFET. Основною перевагою цієї структури є посилена процедура виготовлення шляхом усунення *p-n*-переходів. У даній роботі досліджено вплив довжини каналу та матеріалів високої щільності на підпорогові характеристики безперехідних циліндричних польових транзисторів (JLTMCSG-MOSFET) з високоелектричними діелектриками затворів та пробними матеріалами з використанням двовимірної аналітичної моделі. Ця модель базується на розв'язанні рівняння Пуассона в безперервних циліндричних областях використовуючи метод суперпозиції, де для отримання точного розв'язку використовувалися ряд Фур'є-Бесселя та метод сепарації. Продуктивність JLTMCSG-MOSFET малої потужності досліджено з точки зору розподілу поверхневого потенціалу, електричного поля, підпорогового струму, зниження індукованого стоком бар'єру, підпорогового нахилу і порогової напруги. Це дослідження проводиться в широкому діапазоні довжин каналів і з використанням високоелектричних затворів. Дане дослідження підтверджує, що використана аналітична модель корисна не тільки для моделювання схем, а й для проектування та оптимізації пристроїв як для логічних, так і для аналогових радіочастотних схем.

Ключові слова: Безперехідні MOSFET, Ефект довжини каналу, Діелектрики з високою проникністю, Моделювання нанорозмірних пристроїв.