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INVESTIGATION OF A HYBRID REDUNDANCY IN THE FAULT-TOLERANT SYSTEMS

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ABSTRACT

Context. Structural redundancy is one of the main ways to create highly reliable devices and systems for critical applications. The object of the study was hybrid redundancy in the Fault-Tolerant Systems, for example in aerospace hardware exposed to radiation.

Objective. The goal of the work is the calculation of the complexity and probability of failure-free operation of digital circuits with hybrid redundancy combining tripling, deep tripling, and quadding. The comparison shows that tripling is not always better than a circuit without redundancy over a sufficiently large time interval. Good results are obtained by tripling with three majority voters and deep tripling, but the latter significantly increases the time delay of the signal. The greatest gain in reliability provides quadding at the transistors level, but it is not always possible due to the restrictions of Mead-Conway, in addition, the delay at least is doubled. The article describes proposed method of the combined redundancy taking into account the necessary hardware costs and time delay.

Method. Determining the complexity in the units of the conditional number of transistors and maximum signal path from the input to the output in the number of transistors, as well as using the Weibull distribution to estimate the probability of failure-free operation. Simulation of proposed hybrid redundancy in the system NI Multisim by National Instruments Electronics Workbench Group. The failure-free operation probability estimation in the computer mathematics system MathCad.

Results. Expressions are obtained for the estimates of complexity, time delay and probability of failure-free operation of redundant digital circuits; curves are built in the Mathcad. Simulation confirms the performance of the proposed redundancy options.

Conclusions. The conducted studies allowed us to establish the effectiveness of hybrid redundancy to improve the reliability and the radiation resistance of the digital circuits.

KEYWORDS: Redundancy, Triple Modular Redundancy, Quadding Redundancy, Failure-Free Operation Probability.

ABBREVIATIONS

TMR is a Triple Modular Redundancy;
QR is a Quadding Redundancy;
RBD is a Reliability Block Diagram;
DT is a Deep Triple Modular Redundancy;
HR is a Hybrid Redundancy;
DNF is a Disjunctive Normal Form;
CNF is a Conjunctive Normal Form.

NOMENCLATURE

λ is a failure rate of one transistor (1 / hour);
t is an operation time in hours;
α is a Weibull distribution coefficient;
$e^{-\lambda \cdot t^{\alpha}}$ is a failure-free operation probability of the circuit without redundancy;
P_{EM} is a failure-free operation probability of the circuit with exist redundancy;
n is a common amount of the transistors in device without redundancy;
n_{EM} is a common amount of the transistors in device with exist redundancy;
n_{HR} is a common amount of the transistors in device with proposed redundancy;
τ_{EM} is a conditional time delay of the device with exist redundancy;
τ_{HR} is a conditional time delay of the device with proposed redundancy;
P_{HR} is a failure-free operation probability of the circuit with proposed redundancy;
r is a share of the transistors for QR;
e is an amount of the parryable faults;
k is an amount of the DT layers.

INTRODUCTION

Fault-Tolerance Theory is the relatively young Theory was formed from the Von Neumann works [1] to Avizenis A. [2] and further to modern researchers [3–6].

Fault-Tolerance Systems are very important in aerospace, medical, nuclear power plant, military hardware [2, 3]. Under the radiation in Integrated Circuits, two types of failures are observed [7]: some occur because of accumulation of a dose of radiation, others occur because of hitting a single particle. The first type of failure includes, for example, an increase in delays inside the Integrated Circuits or a change in logic levels. The second type of failure is called single events. Such events include, for example, the Single Event Latch. Next is Single Event Gate Rupture, Single Event Transient, Short-term state change of the logic output. Single Event Upset reversibly changes the state of the memory register, RAM, or flip-flop. Single Event Hard Error irreversibly changes the state of the memory register, RAM, or flip-flop and others.

In Radiation Hardened by Design [8–10] device are used special circuit and technological methods to increase radiation resistance for example Passive Fault-Tolerant and Active fault-tolerance technique [11]. For example,

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Passive Fault-Tolerant Systems uses Triple Modular Redundancy, Deep Triple Modular Redundancy, Quadding Redundancy. Similar technologies are currently being applied at the FPGA level and provides radiation protection too [12,13].

The object of study is the Passive Fault-Tolerant Systems based on RHBD Radiation Hardened by Design CMOS circuits or pass transistors circuits.

The subject of study is the Triple Modular Redundancy, Deep Triple Modular Redundancy and Quadding Redundancy methods for parrying radiation faults (single events) by Hybrid Redundancy.

The known sampling methods [4–6, 12–16] not uses hybrid types of the Triple Modular Redundancy, Deep Triple Modular Redundancy / Quadding Redundancy.

The purpose of the work is to establish Hybrid Redundancy capabilities at the CMOS transistor level.

1 PROBLEM STATEMENT

Given: $P_{EM}, n_{EM}, \tau_{EM}$ according existing methods of Fault-Tolerant Systems, Radiation Hardened by Design Systems: Triple Modular Redundancy (TMR), Deep Triple Modular Redundancy (DT), or Quadding Redundancy (QR).

In the literature [1–16], the problems of Hybrid Redundancy (HR) are not fully covered.

It is required: investigate the effectiveness of HR in the sense of complexing TMR, DT, QR and obtain P_{HR},

$$n_{HR}, \quad \tau_{HR}, \quad \delta n = n_{EM} - n_{HR}, \quad \Psi = \frac{P_{HR} - e^{-\lambda \cdot t^{\alpha}}}{\delta n}$$

according proposed HR.

2 REVIEW OF THE LITERATURE

The Radiation Hardened by Design methods [8–10] for parrying IC radiation faults (single events), are divided into parrying methods to reversibly changes and parrying methods to irreversibly changes.

Radiation resistance is the property of equipment, component elements and materials to perform their functions and maintain parameters within the established standards during or after ionizing radiation. To create radiation-resistant microcircuits, commercial technologies are used, for example, Silicon-on-insulator, which excludes thyristor effects. Well proven technology silicon on sapphire. The Radiation Hardened by Design methods includes parrying Single Event Upset cells of static random access memory SRAM by means of special duplication – Dual Interlocked Storage Cell [14]. For parrying faults, it is used TMR [13], NN-Transistor Structure for Defect-Tolerance at the Nanoscale [15], for example QR. TMR for the A, B, C one bit channels [3] shows Fig. 1.

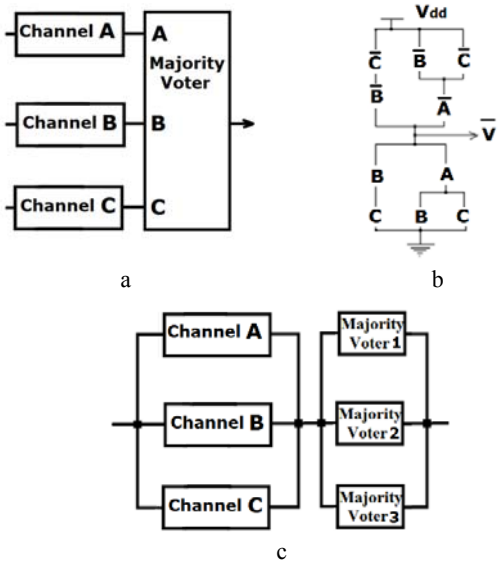

Figure 1 – TMR: a – Tripled Circuit (Channels A, B, C); b – Conditional CMOS Mirror Majority Vote Circuit (Decision Circuit); c – Conditional TMR RBD with three Majority Voter

Channels A, B, C (Fig. 1 a, c) can be single output circuits. If there are several outputs, then each requires its own Majority Vote. CMOS Mirror Majority Vote Circuit (Decision Circuit) has three A, B, C p-type transistors in the part of the circuit connected to the power supply Vdd, and three transistors of n-type in the part of the circuit connected to the Ground. Conditional TMR RBD shows logic OR of the A, B, C, bur real logic functions V (NOT V) of the Majority Vote Circuit (for the p-type transistors) are as follows:

$$\begin{gathered} V(ABC) = AB \vee AC \vee BC, \\ \overline{V}(ABC) = \overline{AB \vee AC \vee BC} = \\ (\overline{AB})(\overline{AC})(\overline{BC}) = (\overline{A} \vee \overline{B})(\overline{A} \vee \overline{C})(\overline{B} \vee \overline{C}) = \\ = \overline{A}\,\overline{B} \vee \overline{A}\,\overline{C} \vee \overline{B}\,\overline{C}. \end{gathered} \quad (1)$$

Thus, any error (radiation faults) in one of the channels A, B, C (Figure 1a, formulas 1) will not lead to an incorrect result if there is no radiation fault in the Majority Voter. In order to take into account the possibility of failure of Majority Voter, it also mast be triple (Figure 1b). In this case, the failure of one channel and one Majority Voter is allowed. This TMR is more than 300% redundancy, since Majority Voters, three more power sources and tripling of communication lines are needed. It increases reliability in a logical sense. However, it is required a quantitative assessment of reliability in the sense of probability theory

Weibull distribution [3] is most suitable for describing the reliability of circuits under conditions of radiation exposure. Let "12" is a complexity of the Majority Vote Circuit in amount of the transistors (Fig.1–b); $1 \le \alpha \le 2$. Formula (2) describes failure-free operation probability of the TMR system (Fig. 1 a).

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$$P_{tmr} = (3 \cdot e^{-2 \cdot (n) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (n) \cdot \lambda \cdot t^{\alpha}}) e^{-(12) \cdot \lambda \cdot t^{\alpha}}. \quad (2)$$

With the Majority Voters tripling (Fig. 1 c), we get formula (3)

$$P_{tmr3} = (3 \cdot e^{-2 \cdot (n) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (n) \cdot \lambda \cdot t^{\alpha}}) \times \times (3 \cdot e^{-2 \cdot (12) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (12) \cdot \lambda \cdot t^{\alpha}}). \quad (3)$$

Comparison of (3) and (2) shows great efficiency, of course at the expense of high costs. Thus, TMR can parry only one (2) or two (3) radiation failures in one channel or in one Majority Voters. TMR delay increases due to Majority Vote Circuit delay (two transistors delay of the CMOS Mirror Majority Vote Fig. 1b + additional one transistor delay of the CMOS NOT).

The analysis shows that the probability (2), (3) of increases with a larger number of parried failures and decrease failure rate of the channels A,B,C. This approach is implemented in Deep Triple Modular Redundancy (DT)

DT (k-layer tripling) shows Fig. 2 and is described by formula (4)

$$P_{dt} = [3e^{-2n\frac{\lambda}{k}t^{\alpha}} - 2e^{-3n\frac{\lambda}{k}t^{\alpha}}]^k \times \times [3e^{-2 \cdot 12\lambda\, t^{\alpha}} - 2e^{-3 \cdot 12\lambda\, t^{\alpha}}]^k, \quad (4)$$

$n\lambda$ – the failure rate of the entire channel.

With such DT (k-layer) redundancy (Fig. 2), radiation failures is parried in each k layer of the generalized channels A,B,C and in each generalized Majority Vote. This further increases costs and the time delay in the circuit due to k Majority Vote. However, the effectiveness of (4) is much higher than (2) and (3).

In common case it is parrying e radiation fault from $2e+1$, where e – number of the failures (errors), we get formula (5).

$$P(t, e, \lambda, \alpha) = \sum_{i=0}^{e} C_{2e+1}^{i} \left\{ e^{-[(2e+1)-i] \cdot \lambda \cdot t^{\alpha}} \cdot \left(1 - e^{-\lambda \cdot t^{\alpha}}\right)^{i} \right\}. \quad (5)$$

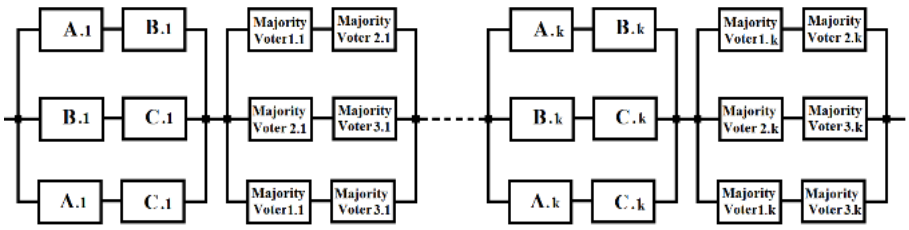
Limit of the triple redundancy depth at the present technology level – is one element (gate, flip-flop or SRAM cell), transistors cannot be tripled. However, they can be quadded [15]: A,B,C,D – four copies of one transistor for e=1 (Fig. 3).

We see (Fig. 3) that with any radiation failure (=1,= 0, NOT) of one transistor (value A=B=C=D), the logic function does not change.

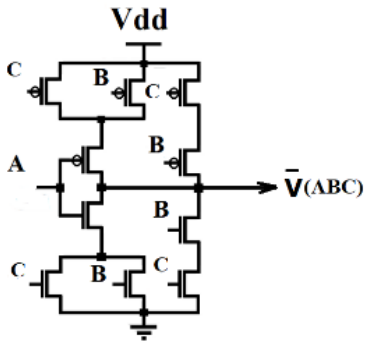
QR on transistors level does not required Majority Voters because it is implemented implicitly by connecting transistors. Therefore, we get parrying any fault of one transistors from four transistors for the each transistors in circuit unlike (2)–(5) – expression 6.

$$P(t)_{qr} = [e^{-4 \cdot \lambda \cdot t^{\alpha}} + 4 \cdot e^{-3 \cdot \lambda \cdot t^{\alpha}} (1 - e^{-\lambda \cdot t^{\alpha}})]^n. \quad (6)$$

However, redundancy increases even more – up to 400% percent with e=1.



a



b

Figure 2 – DT (k-layer) a – Real RBD; b – Real CMOS Mirror Majority Vote Circuit

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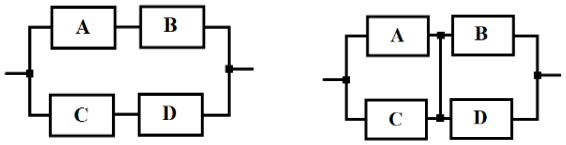

a b

Figure 3 – QR circuits: a – DNF option; b – CNF option

In common, case parrying any faults, one of the e transistors from $(e+1)^2$ we get formula (7).

$$P_{(e)\,from\,(e+1)^2}(t)=\sum_{i=0}^{e}C^{i}_{(e+1)^2}\{e^{-[(e+1)^2-i]\cdot\lambda\cdot t^{\alpha}}\cdot(1-e^{-\lambda\cdot t^{\alpha}})^{i}\}. \quad (7)$$

At e=2 we get 900% redundancy. At e=3 we get 1600% redundancy. Moreover, there are restrictions on the number of series-connected transistors. This is a lack of QR. Therefore, we restrict ourselves to e = 1. Besides quadding circuit time delay increases more than $\frac{(e+1)^2}{e}$ times compared to the original circuit (Fig. 3, expression 6, 7). Thus, each method has its advantages and disadvantages. It is advisable to determine the conditions for their effective combination. Based on the above, an hybridization of known methods of introducing redundancy is proposed (Hybrid Redundancy, HR).

3 MATERIALS AND METHODS

Hybrid Redundancy estimates we are obtained by possible modifying the formulas (1)–(7). First, it is necessary to determine the circuit complexity, time delay and possibly other estimates for the proposed HR. To do this, we will perform modeling of typical CMOS circuits and circuits used in the FPGA, which characterize the basic set of digital elements.

Simulation of the QR, TMR, HR is performed in the system NI Multisim by National Instruments Electronics Workbench Group.

Then it is necessary to determine failure-free operation probability of the different proposed and experimentally confirmed HR variants.

The first variant of combining redundancy P_{tmr34} is proposed: only Majority Voter (12 transistors, with additional inverter not specified in Fig. 2b) is quadded – formula (8):

$$P_{tmr34}=(3\cdot e^{-2\cdot(n)\cdot\lambda\cdot t^{\alpha}}-2\cdot e^{-3\cdot(n)\cdot\lambda\cdot t^{\alpha}})\times \times[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{12}, \quad (8)$$

In expression (8) part $(3\cdot e^{-2\cdot(n)\cdot\lambda\cdot t^{\alpha}}-2\cdot e^{-3\cdot(n)\cdot\lambda\cdot t^{\alpha}})$ is tripled system including n transistors (λ is the failure rate of one transistor, 1/hour) in each A, B, C channels (Fig. 1a). Part $[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{12}$ presents quadded Majority Voter (Fig. 2 a).

The second variant P_{tmr34g} : Quadding of the Majority Voter transistors and r-part of the n transistors; tripling of the gates with n-rn transistors is – formula (9):

$$P_{tmr34g}=(3\cdot e^{-2\cdot(n-rn)\cdot\lambda\cdot t^{\alpha}}-2\cdot e^{-3\cdot(n-rn)\cdot\lambda\cdot t^{\alpha}})\times \times[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{12+rn}. \quad (9)$$

Take into account that rn transistors are quadded so rn is added to the number of transistors in the Majority Voter (12 + rn). The same value rn is deducted from the total number n in tripled part.

This option does not take into account the requirements of the Mead-Conway [17]. It is assumed that they are respected. The third variant P_{dtqr} uses deep tripling at k(1–r) levels and nr quadding, Majority Voters are quadded:

$$P_{dtqr}=[3e^{-2n\frac{\lambda}{k}t^{\alpha}}-2e^{-3n\frac{\lambda}{k}t^{\alpha}}]^{k-kr}\cdot \cdot[3e^{-2\cdot12\lambda\,t^{\alpha}}-2e^{-3\cdot12\lambda\,t^{\alpha}}]^{k-kr}\cdot \cdot[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{nr}. \quad (10)$$

In formula (10) subexpression $[3e^{-2n\frac{\lambda}{k}t^{\alpha}}-2e^{-3n\frac{\lambda}{k}t^{\alpha}}]^{k-kr}$ is the failure-free operation probability of the DT part of the system, $[3e^{-2\cdot12\lambda\,t^{\alpha}}-2e^{-3\cdot12\lambda\,t^{\alpha}}]^{k-kr}$ is failure-free operation probability of the k(1–r) Majority Voters according (4).

The fours variant is tripling of the quadded circuit $P_{tq(t)}$

$$P_{tq(t)}=(3\cdot e^{-2\cdot[-\frac{\ln([e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{n})]\cdot t^{\alpha}}{t^{\alpha}}}- -2\cdot e^{-3\cdot[-\frac{\ln([e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{n}}{t^{\alpha}}]\cdot t^{\alpha}})\times \times[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{12}, \quad (11)$$

Note $-\frac{\ln([e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{n}}{t^{\alpha}}$ is the failure rate of the quadded part. Therefore, the expression (11) is not simplified. Second element of the (11) is equal the second element of the (8).

The next variant $P_{tmr34gt}$ – part of the gates with n transistors is quadding (gates with rn transistors); tripling of the gates with n-rn transistors + Majority Voter is quadding – formula 12.

$$P_{tmr34gt}=(3\cdot e^{-2\cdot[(n-rn)\cdot\lambda-\frac{\ln([e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{rn})]\cdot t^{\alpha}}{t}}- -2\cdot e^{-3\cdot[(n-rn)\cdot\lambda-\frac{\ln([e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{rn}}{t}]\cdot t^{\alpha}})\times \times[e^{-4\cdot\lambda\cdot t^{\alpha}}+4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{12}, \quad (12)$$

So formula (12) is combined expression (9) and (11). Failure-free operation probability according existing and proposed expressions is estimated in the computer mathematics system MathCad. Hardware conditional costs in number of the transistors, conditional time delay are corrected taking into account experimental resalts.

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4 EXPERIMENTS

Let us perform simulation of the base CMOS logic gates with QR. For example simplest CMOS NOT QR (CNF option) gate static simulation shows Fig. 4.

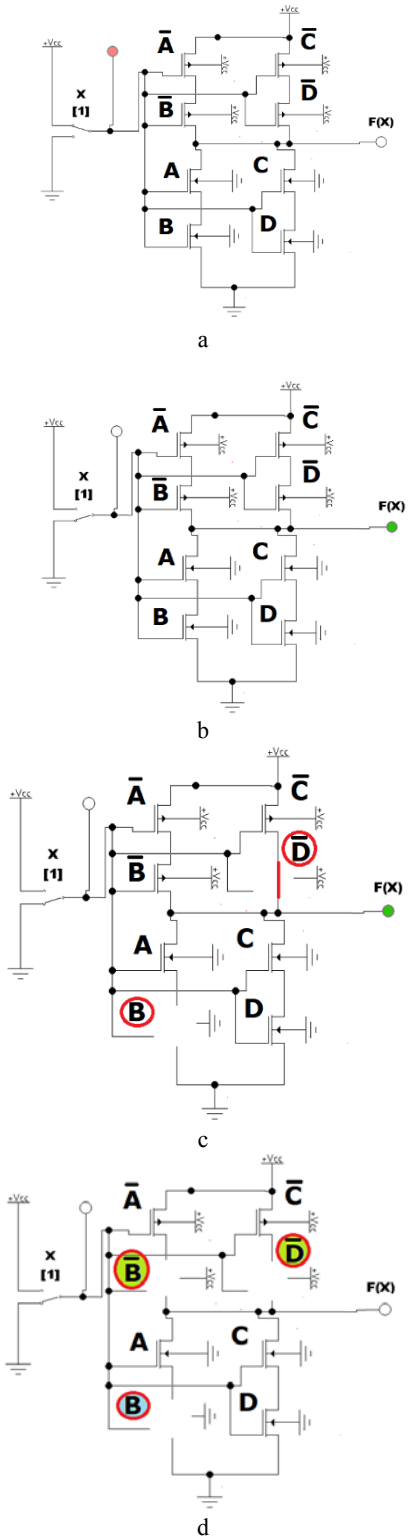

Figure 4 – QR of the CMOS NOT Gate static simulation: a – x=1; $F(x)$=0; b – x=0; $F(x)$=1; c – defaults B, $\overline{D}$; d – default CMOS NOT at defaults B, $\overline{B}$, $\overline{D}$.

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Fig. 4 corresponds to QR DNF option (Fig. 3 a). QR parry any single radiation defect in A,B,C,D or/and $\overline{A},\overline{B},\overline{C},\overline{D}$ (Fig. 4 c). The number of transistors quadruples from two to eight and the delay in the number of transistors in the path from Power supply twice.

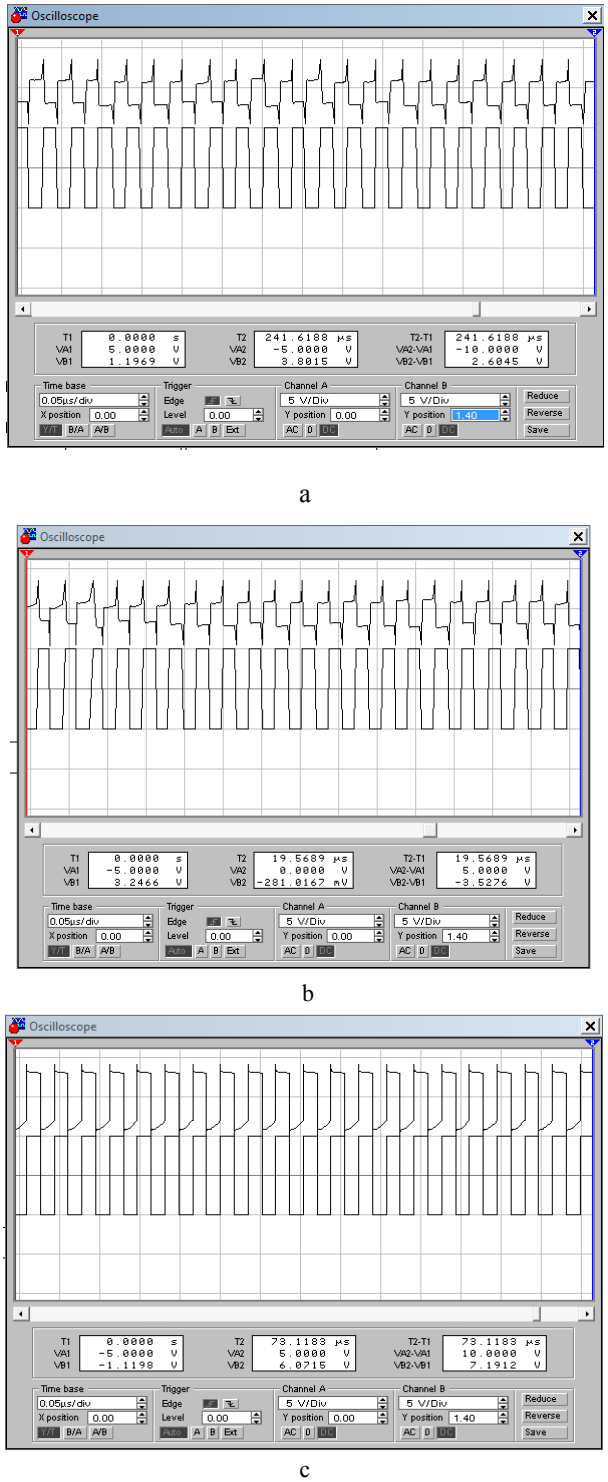

Figure 5 – QR CMOS NOT Gate dynamic simulation: a – Quad NOT normal waveform; b – Single Fault – Quad NOT correct waveform; c – Two Faults – Quad NOT defect waveform

Since the NOT Gate have a single transistor in each of the two parts of the circuit, the QR leads to a twofold increase of the time delay so the Mead-Conway constraints [15] are performed.

It is easy to see that the QR in the logical gate 2NAND (2NOR) will lead to a path of a maximum of four transistors. These restrictions allow for a series of no more than four transistors. As a rule, we are talking even about three transistors. For example, in FPGA, after every three transistors, a signal-level restorer is installed. Four transistors in a row are present, for example, in 4NAND (4NOR). It is clear that the direct QR of 3NAND (3NOR) is unacceptable, the decomposition by 2NAND (2NOR) is required. Fig. 5 shows dynamic simulation results of the QR NOT gate without faults – a; with single fault, (e=1) – b; with two faults, (e=2) – c.

Fig. 5 b, c confirms that with one fault (for example – default B, $\overline{D}$ Fig.4 c) the circuit functions correctly, the circuit is not operational if two transistors fail in one part of the circuit (for example – default A,B Fig.4).

At the same time, the Majority Voter (Fig. 2 b) performs NOT function of the three channels with the same time delay, but the cost is ten transistor.

LUT FPGA – is the universal logical module or functional generator or multiplexer $2^n \rightarrow 1$, for example at n=1: SRAM0 is the F(0), SRAM1is the F(1).

A comparison QR with TMR shows the preference QR for energy consumption, for example as shown Fig. 6 for the TMR and QR LUT FPGA (n=1).

Fig. 6 a, b does not take into account additional inverters for the output and inputs, which are taken into account in the Fig. 6 c.

Simulation of the LUT-2 and the measuring of the power consumption of the LUTs shows Fig. 7.

Similarly, was performed the simulation and investigation of the redundancy SRAM cell, D-flip-flop, 3-state buffer.

Then let us build Failure-free operation probability curves in the computer mathematics system MathCad based on the results of circuits simulation.

5 RESULTS

The simulation results of the TMR and/or QR FPGA's basic elements confirmed the possibility of the proposed combined redundancy. As it turned out, the QR gives a gain in power consumption (Fig. 7 b).

Comparative curves of the original CMOS NOT circuit failure-free operation probability and TMR, TMR3, QR shows Fig. 8 – a, b. Fig. 8 – c, n=20, – d, n=100 graphically illustrates the QR advantage with increasing number of transistors n.

Increasing of the failure-free operation probability by using hybrid redundancy demonstrates Fig. 8 – e, n=50; r=0.5; k=10; – f, n=100; r=0.4; k=7. The unit specific probability (Formula 13) is obtained taking into account the costs in number of the transistors (Table 1).

$$\Psi_{P_\xi} = \frac{P_\xi - e^{-n\lambda \cdot t^\alpha}}{\delta n}. \quad (13)$$

Charts are shown on Fig. 8 – g, t=50; r=0.7; k=10; – h, t=10; r=0.5; k=7.

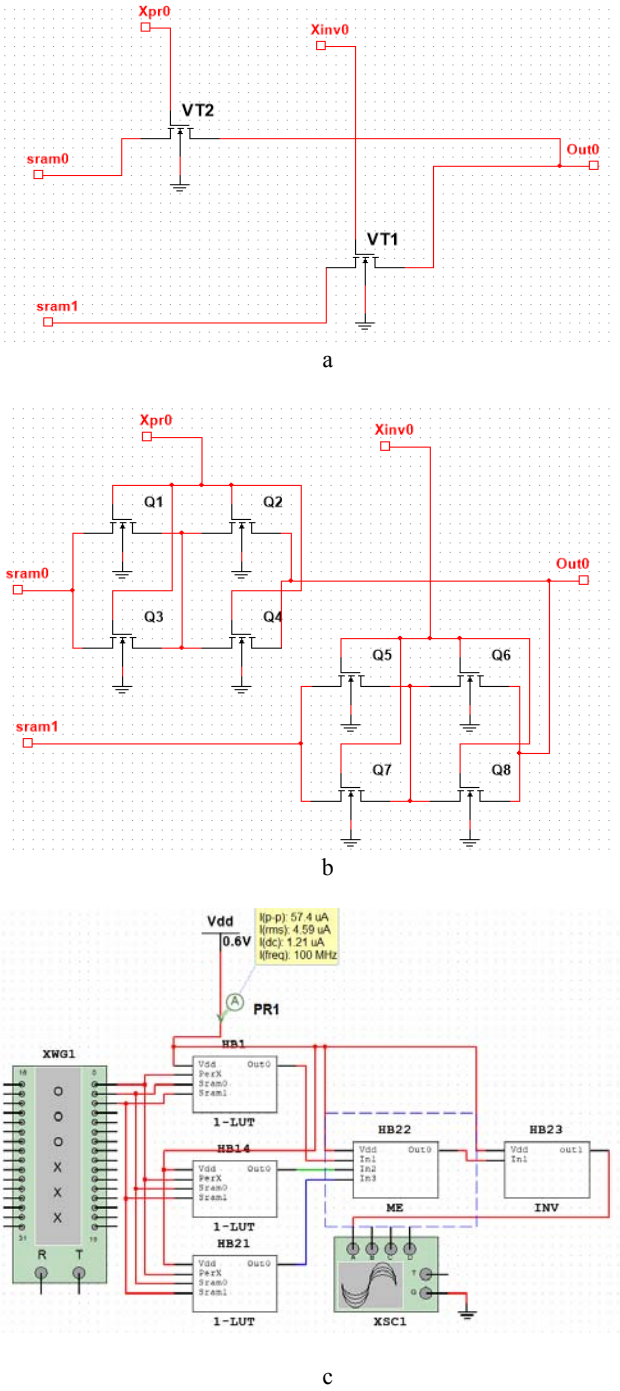

Figure 6 – Experiment with LUT FPGA (n=1): a – LUT-1; b – QR LUT-1 and c – LUT-1 TMR

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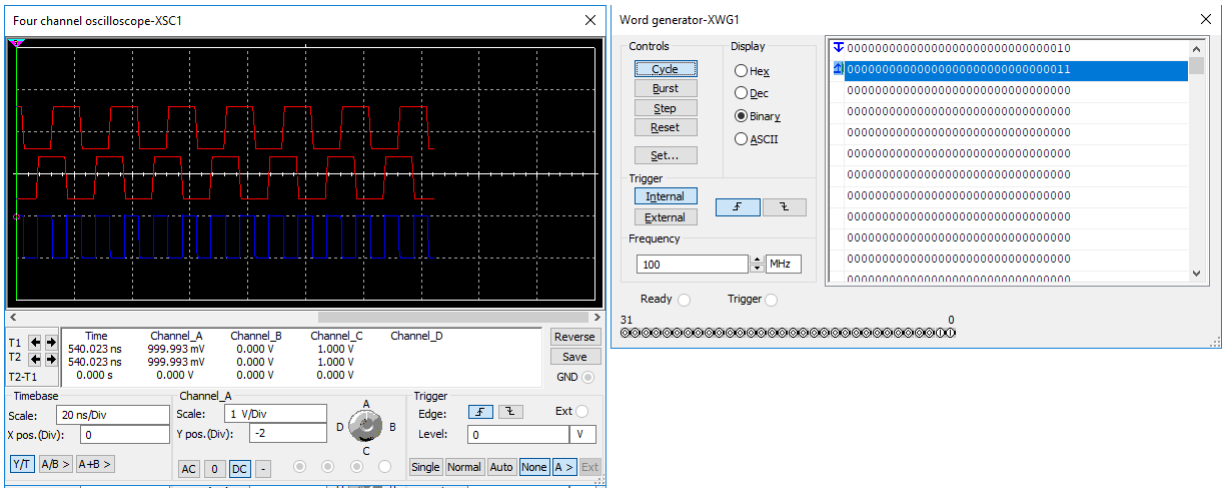
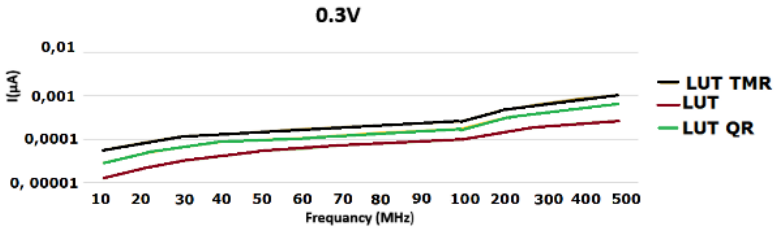


a



b

Figure 7 – LUT-2 simulation: a – XOR waveform; b – a comparison power consumption of the LUTs at 0,3 V Power Supply

Table 1 – The hardware and time costs of the QR/TMR and HR

№	Failure-free operation probability symbol	Hardware conditional costs in number of the transistors	Conditional time delay	Note
1	P_{tmr}	$3n+12$	τ_n+2	TMR, Excluding additional power supplies; τ_n – time delay of the circuit with n transistors; 2– time delay of the Majority Voter
2	P_{tmr3}	$3n+36$	τ_n+2	TMR3, Majority Voters tripling
3	P_{dt}	$3n+36k$	τ_n+2k	DT, Majority Voters tripling
4	P_{qr}	$4n$	$2\tau_n$	QR, Without taking into account the decomposition
5	P_{tmr34}	$3n+48$	τ_n+4	HR (TMR+QR) Majority Voter
6	P_{tmr34g}	$3n(1-r)+4nr+48$	$\tau_{n(1-r)}+2\tau_{nr}+4$	HR (TMR+QR) Majority Voter
7	P_{dtqr}	$3n(1-r)+4nr+48k$	$\tau_{n(1-r)}+2\tau_{nr}+4k$	HR (DT+QR)
8	$P_{tq(t)}$	$12n+48$	$2\tau_n+2$	HR (TMR+QR)
9	$P_{tmr34gt}$	$12n(1-r)+4nr+48$	$2\tau_{n(1-r)}+2\tau_{nr}+4$	HR (TMR+QR)

6 DISCUSSION

As it evident from the Fig. 8 – a,b with a small "n", the TMR P_{tmr} is worse than the non-redundant circuit. TMR P_{tmr3} wins only to probability 0.99 (n=2, t=60), and then it becomes lower than the non-redundant circuit. At the same time, QR P_{qr} is better any TMR. However, and G falls below after a probability of about 0.6 (t about 800). With an increase in n (20, 100) QR wins over the entire time interval (Fig. 8 – c, d).

The direct introduction of QR into logical elements with e = 1 is possible only for two-seat operations, and for the implementation of the others logic gates decomposition is necessary, which increases the complexity and delay.

$P_{tq(t)}$ allows to achieve maximum reliability (Fig. 8 – e, f), but this requires a very large redundancy (Table 1).

Quadding "not more expensive" than CMOS tripling (Table 1) in case a large number of outputs m, since each

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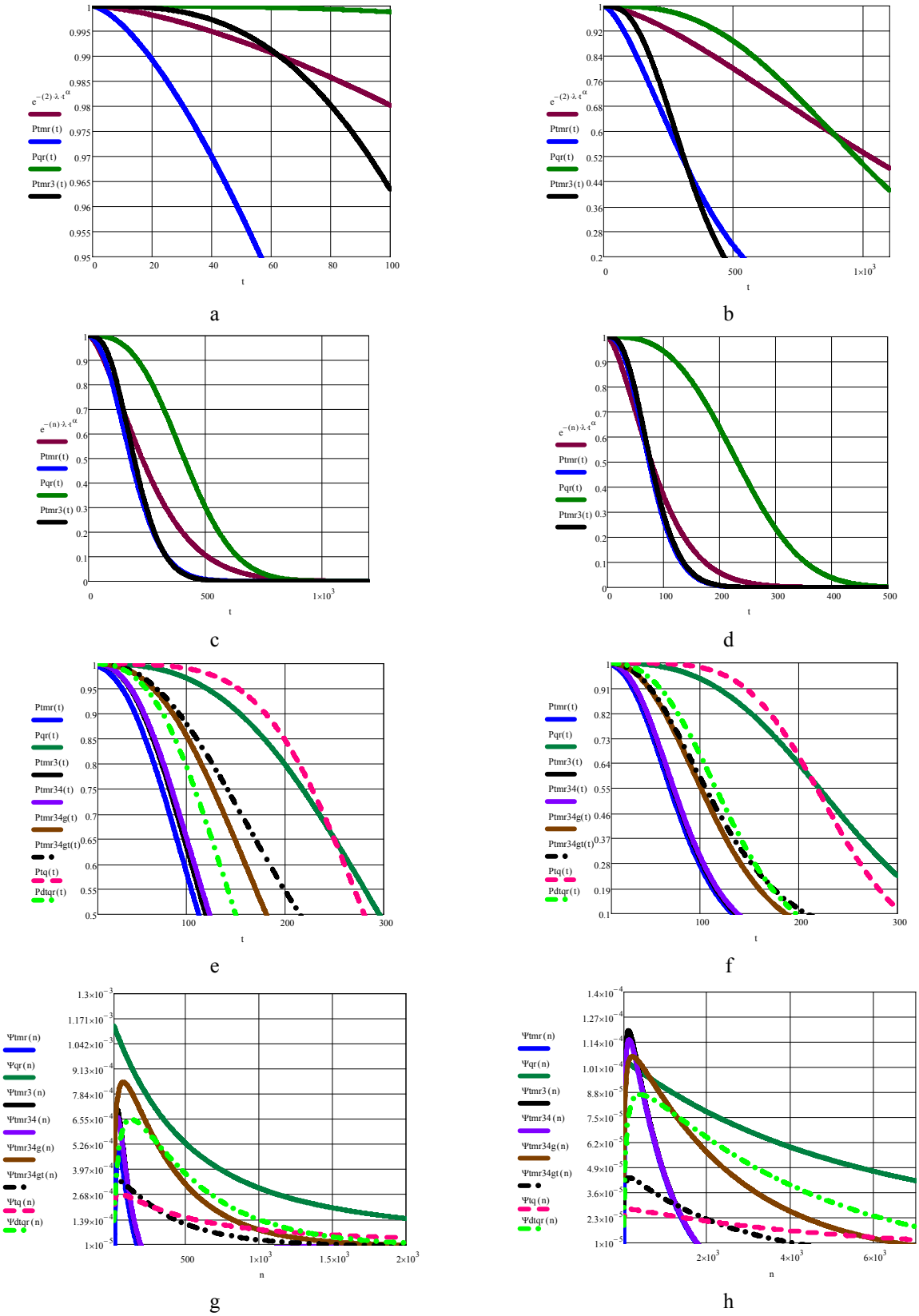

a b c d e f g h

Figure 8 – Failure-free operation probability of the TMR, QR, HR:
a – n=2, t=0…100; b – n=2; t=0…1000; c – n=20; d – n=100; e – n=50 r=0,5; k=10 ; f – n=100; r=0,4; k=7; g – t=50; r=0,7; k=10;
h – t=10; r=0.5; k=7; $\lambda = 10^{-5}, \alpha = 1.5$

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of them must has TMR Voter (12 transistors), that determined by the formula (8):

$$4n \le 3n + 12m \Rightarrow 1 \le 12\frac{m}{n}. \quad (14)$$

For example 2NOR (2NAND) gate has n=four, so we get 16 transistors (QR) against 24 (TMR). In addition, time delay TMR 2NOR (2NAND) in amount of the transistors is five, time delay QR 2NOR (2NAND) is equal four. That is, with a small n there is an advantage in terms of complexity and delay even at *m*=1! However, TMR, unlike QR, takes into account the failure of one of the three power sources. However, it can be shown that K has the ability to connect a backup power source.

It is easy to see that redundancy at the circuit level and even more so at the channel level is worse than redundancy at the level of individual transistors.

Failure-free operation probability of quadding channel requires specific CMOS voter circuit (for example Fig. 4). Quadding transistors (6) better than quadding circuits (15) and channels (16):

$$P(t)_{4-circuit} = [e^{-4\cdot n\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot n\lambda\cdot t^{\alpha}}(1-e^{-n\lambda\cdot t^{\alpha}})]. \quad (15)$$

$$P(t)_{4-channel} = [e^{-4\cdot n\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot n\lambda\cdot t^{\alpha}}(1-e^{-n\lambda\cdot t^{\alpha}})]\times \times[e^{-4\cdot\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]. \quad (16)$$

Option (15) for time delay is equivalent to (6), although it is possible that this option (15) is preferable technologically, this requires further study of the corresponding sizes of the crystals areas. At the same time, (15) requires compliance with the Mead-Conway restrictions, and (16) does not.

However, channel quadded-structure (16) much worse than quadded-transistor (6) and tripling (2), (3), (4).

Taking into account the restrictions of Mead-Conway, DT with partial QR P_{dtqr} (Fig. 8 – e, f) is most preferable compared to clean redundancy (Fig. 8 – c, d). The specific unit probability of the P_{dtqr} is most preferable too (Fig. 8 – g, h).

However, P_{dtqr} requires a significant increase of the latency "input-output" which may be unacceptable in some cases.

Therefore useful TMR-QR P_{tmr34g} (Fig. 8 – g, h) in the case of strict limitations in the time delay.

CONCLUSIONS

The problem of creating Passive Fault-Tolerant Systems with Hybrid Redundancy is urgent, as known types of redundancy in some cases do not allow achieving the required reliability in radiation conditions.

The scientific novelty of obtained results is that the proposed method uses a combination of Triple Modular Redundancy, Deep Triple Modular Redundancy, Quadding Redundancy, taking into account the necessary hardware costs and time delay. The resulting estimates and expressions allow finding the desired and optimal option in specific conditions.

The practical significance of obtained results lies in the fact that the simulation of the proposed options for redundancy confirmed their effectiveness, which allows you to create systems with a new level of reliability and radiation resistance

Prospects for further research are to study the problem of optimal Quadding Redundancy decomposition for the satisfaction of the Mid-Conway restrictions in the modern FPGA's LUTs [18].

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ДОСЛІДЖЕННЯ ГІБРИДНІ НАДЛИШКОВОСТІ В ВИДМОВОСТОЙКИХ СИСТЕМАХ

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АННОТАЦІЯ

Актуальність. Структурне резервування є одним з основних способів створення високонадійних пристроїв та систем для критично важливих додатків. Об'єктом дослідження була гібридна надмірність в відмовостійких системах, наприклад, в аерокосмічному обладнанні, яке знаходиться під впливом радіації.

Завдання. Метою даної роботи є розрахунок складності і ймовірності безвідмовної роботи цифрових схем з гібридним резервуванням, що поєднують троїрування (мажоритування), глибоке мажоритування і розчетверування. Порівняння показує, що троїрування не завжди краще, ніж схема без надмірності в кінці чималого інтервалу часу. Хороші результати досягаються шляхом троїрування з трьома мажоритуваннями і глибоке мажоритування, але останнє значно збільшує часову затримку сигналу. Найбільший виграш в надійності досягається за рахунок розчетверування на рівні транзисторів, але це не завжди можливо через обмеження Міда-Конвей, крім того, затримка як мінімум подвоюється. У статті описаний запропонований метод комбінованого резервування з урахуванням необхідних апаратних витрат і часу затримки.

Метод. Визначення складності в одиницях умовного числа транзисторів і максимального шляху проходження сигналу від входу до виходу за кількістю транзисторів, а також використання розподілу Вейбулла для оцінки ймовірності безвідмовної роботи. Моделювання передбачуваної гібридної надмірності в системі NI Multisim від National Instruments Electronics Workbench Group. Оцінка ймовірності безвідмовної роботи в системі комп'ютерної математики MathCad.

Результати. Отримані вирази для оцінки складності, з невеликою затримкою і ймовірністю безвідмовної роботи резервованих цифрових схем; графіки будуються в Mathcad. Моделювання підтверджує ефективність запропонованих варіантів резервування.

Висновки. Проведені дослідження дозволили встановити ефективність гібридного резервування для підвищення надійності і радіаційної стійкості цифрових схем.

КЛЮЧОВІ СЛОВА: надлишковість, троїрування, розчетверування, ймовірність безвідмовної роботи.

УДК 004.93

ИССЛЕДОВАНИЕ ГИБРИДНОЙ ИЗБЫТОЧНОСТИ В ОТКАЗОУСТОЙЧИВЫХ СИСТЕМАХ

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АННОТАЦИЯ

Актуальность. Структурное резервирование является одним из основных способов создания высоконадежных устройств и систем для критически важных приложений. Объектом исследования была гибридная избыточность в отказоустойчивых системах, например, в аэрокосмическом оборудовании, подверженном воздействию радиации.

Задача. Целью данной работы является расчет сложности и вероятности безотказной работы цифровых схем с гибридным резервированием, сочетающих троирование (мажоритирование), глубокое мажоритирование и расчетверение. Сравнение показывает, что троирование не всегда лучше, чем схема без избыточности в конце достаточно большого интервала времени. Хорошие результаты достигаются путем троирования с тремя мажоритарами и глубокое мажоритирование, но последнее значительно увеличивает временную задержку сигнала. Наибольший выигрыш в надежности достигается за счет расчетверения на уровне транзисторов, но это не всегда возможно из-за ограничений Мида-Конвей, кроме того, задержка, как минимум, удваивается. В статье описан предложенный метод комбинированного резервирования с учетом необходимых аппаратных затрат и времени задержки.

Метод. Определение сложности в единицах условного числа транзисторов и максимального пути прохождения сигнала от входа к выходу по количеству транзисторов, а также использование распределения Вейбулла для оценки вероятности безотказной работы. Моделирование предполагаемой гибридной избыточности в системе NI Multisim от National Instruments Electronics Workbench Group. Оценка вероятности безотказной работы в системе компьютерной математики MathCad.

Результаты. Получены выражения для оценки сложности, временной задержки и вероятности безотказной работы резервированных цифровых схем; графики строятся в Mathcad. Моделирование подтверждает эффективность предложенных вариантов резервирования.

Выводы. Проведенные исследования позволили установить эффективность гибридного резервирования для повышения надежности и радиационной стойкости цифровых схем.

КЛЮЧЕВЫЕ СЛОВА: избыточность, троирование, расчетверение, вероятность безотказной работы.

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