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HARDWARE IMPLEMENTATION DESIGN OF A SPIKING NEURON

Abstract. The hardware implementation of an artificial neuron is the key problem of the design of neuromorphic chips which are new promising architectural solutions for massively parallel computing. In this paper an analog neuron circuit design is presented to be used as a building element of spiking neuron networks. The design of the neuron is performed at the transistor level based on Leaky Integrate-and-Fire neuron implementation model. The neuron is simulated using EDA tool to verify the design. Signal waveforms at key nodes of the neuron are obtained and neuron functionality is demonstrated.
Keywords: neuromorphic chip, spiking neuron network, neuron, synapse, weight coefficients, EDA, VLSI.

Introduction. It is well known that a general-purpose central processing unit (CPU) is not well suited for massively parallel computing. At the same time graphics processing units (GPU) are adapted specifically for parallel computations, so they provide significantly higher performance than CPU. That is why neural network operations are performed on arrays of video cards. However, graphics processors are forced to emulate neurons using software tools, which consumes significant processing power.

To increase the performance of computer systems for parallel computations new architectural solutions should be designed. Recently, due to the rapid development of neural network technology, neuromorphic systems that work on the principles of the human brain have become increasingly popular. Such systems are best suited to perform massively parallel computing and provide the highest performance in solving problems traditional for neural network applications. Neuromorphic chips, unlike conventional processors, do not emulate neural networks, but are physically constructed as neural networks. Each chip consists of several hundreds or even thousands of interconnected simple computational elements, that functionally correspond to neurons.

The neuromorphic chip can be constructed as a classic artificial neural network (ANN), or as a pulsed (spiking) neural network (SNN). The latter is more promising

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because its work directly mimics the behavior of a network of biological neurons. In a pulsed neural network, signals between neurons are transmitted in the form of short pulses – spikes. A neuron generates a spike of maximum amplitude when the weighted sum of the input signals exceeds its action potential. Such a neuron can be implemented using existing semiconductor technology, and the neuromorphic chip itself can be made in the form of very large-scale integrated circuit (VLSI) [1].

The key problem of neuromorphic chip design is the hardware implementation of a single neuron. A neuromorphic network can be implemented using either analog or digital circuits. Digital circuit design is generally more simple but analog neuron implementation consumes less energy and requires less area on the silicon chip. There are a large number of papers devoted to the hardware implementations of neurons and neuron networks [2-4]. This paper focuses on an analog implementation of a neuron with digital weight control. Leaky Integrate-and-Fire neuron model [5,6] is used for the design of the neuron on the transistor level and signal waveforms are obtained to verify the functionality of the neuron.

Neuron Circuit Design. Leaky Integrate-and-Fire model of an artificial neuron implementation is consisted of several building blocks shown in Fig. 1. The most significant blocks of the artificial neuron are the synaptic inputs which produce weighted input signals. Like in a real neuron of a human brain, an input signal can be amplified or attenuated corresponding to synaptic weight coefficients. To this end excitatory and inhibitory weight input circuits are provided for each synaptic input block. Post-synaptic signals from all synaptic input blocks are added and formed post-synaptic potential of the neuron using a leaky integrator. The capacitor of the leaky integrator determines the level of the post-synaptic potential and the resistive load ensures that the neuron returns to the relaxed state.

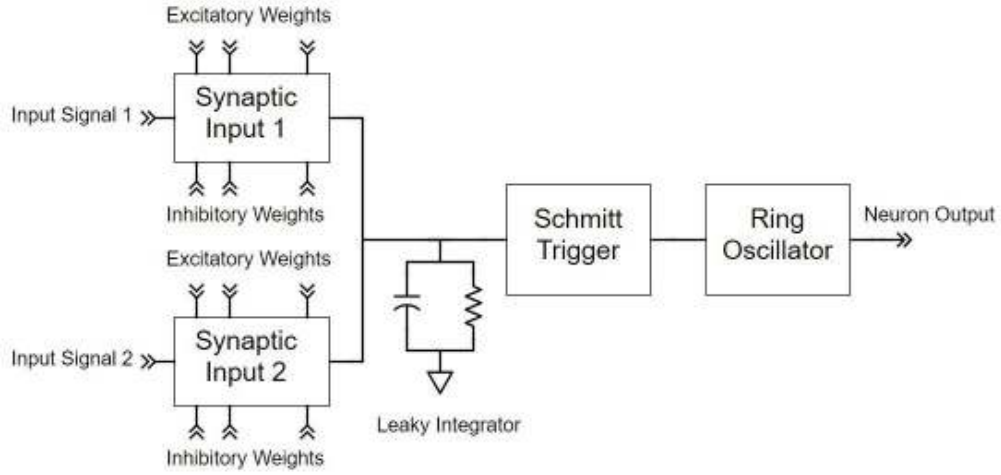

Figure 1 – Block diagram of an analog neuron with two synaptic inputs

Shmitt trigger is used as a neuron activator that performs a threshold activation function. When the post-synaptic potential exceeds a threshold voltage level set by Shmitt trigger, logical "1" is applied to ENABLE input of the ring oscillator. In this case the ring oscillator generates spikes as a neuron output. The neuron does not generate spikes if the post-synaptic potential does not exceed the threshold voltage.

Synaptic Input with Digital Weight Control. A simple synapse realization relies on excitatory and inhibitory circuits consisted of several MOS transistors connected in parallel [5,6] as shown in Fig. 2. Voltages on the gates of these transistors regulate currents from the power source to the output and from the output to the ground. Using only two voltages in the subthreshold regime V_{base} and V_{offset}, where $V_{dd} \geqslant V_{base} > V_{offset}$, we can obtain four variations of voltage level at the post-synaptic output node for three parallel connected MOS transistors in the excitatory circuit. In the same way four voltage levels are obtained for inhibitory circuit using $V_{GND} \leqslant V_{base} < V_{offset}$.

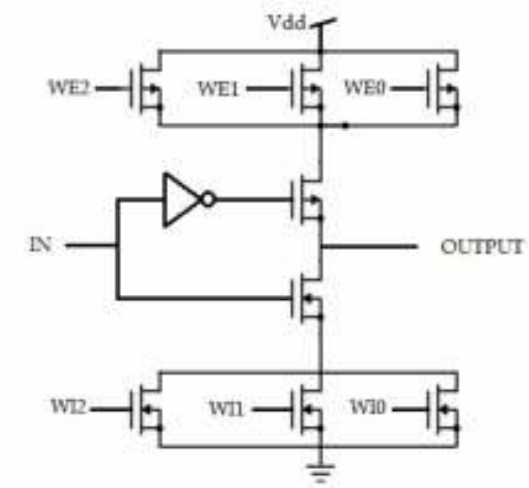

Figure 2 – Synaptic input circuit diagram [5]

To provide four voltage levels at the post-synaptic output node it is enough to use 2-bit numbers for digital weight control. Those numbers regulate the choice of one of two voltage levels applied to transistor gates acting as synaptic weight coefficients. In Fig. 3 it is shown the circuit diagram of a digital voltage control block and a voltage switch block which provide digital control for voltage level applied to the gates. The circuit diagram for the verification of a single synaptic input block is demonstrated in Fig. 4. The results of the verification are shown in Fig. 5 as waveforms at input and output nodes. One can be seen that the voltage level of the post-synaptic potential increases gradually with the rise of the weight number.

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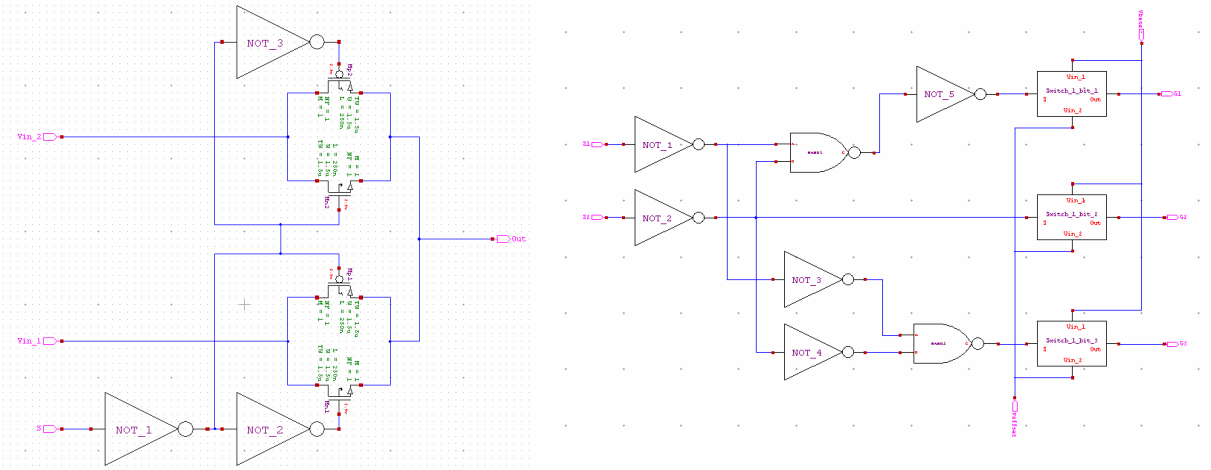

a) b)

Figure 3 – Circuit diagram of a voltage switch block (a) and a digital voltage control block (b)

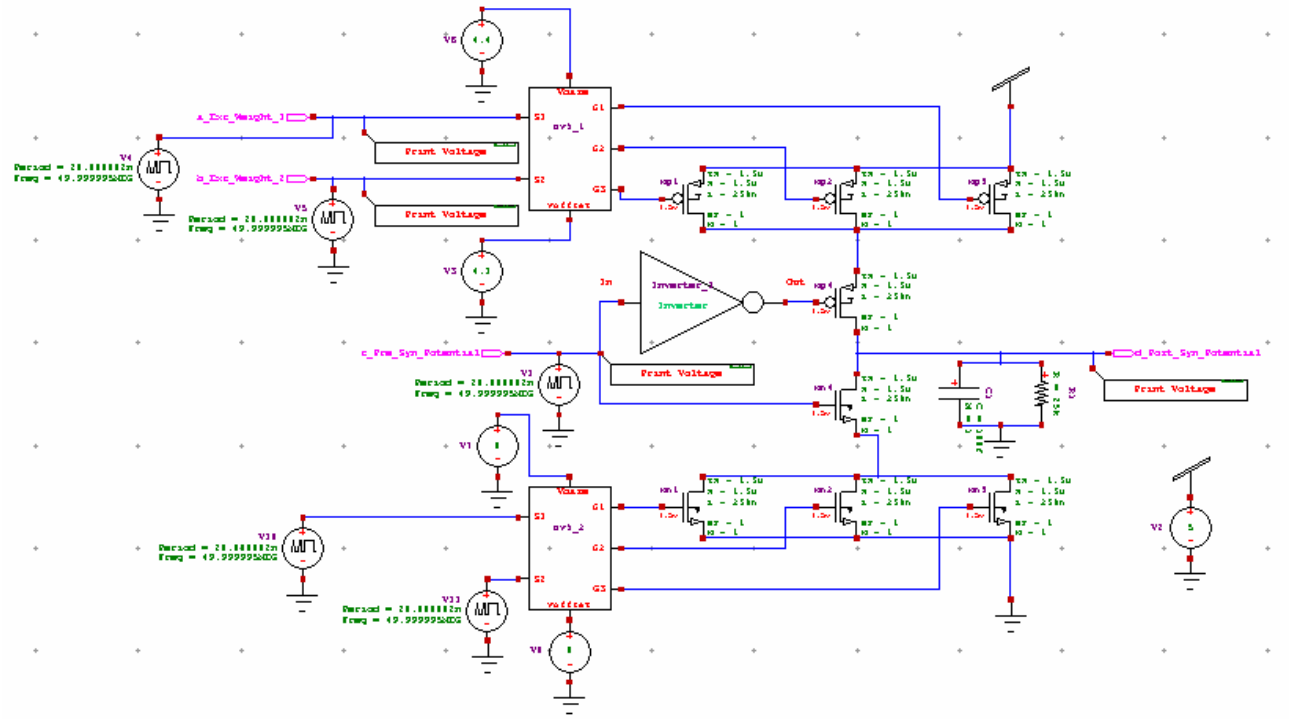

Figure 4 – Circuit diagram for single synaptic input block verification

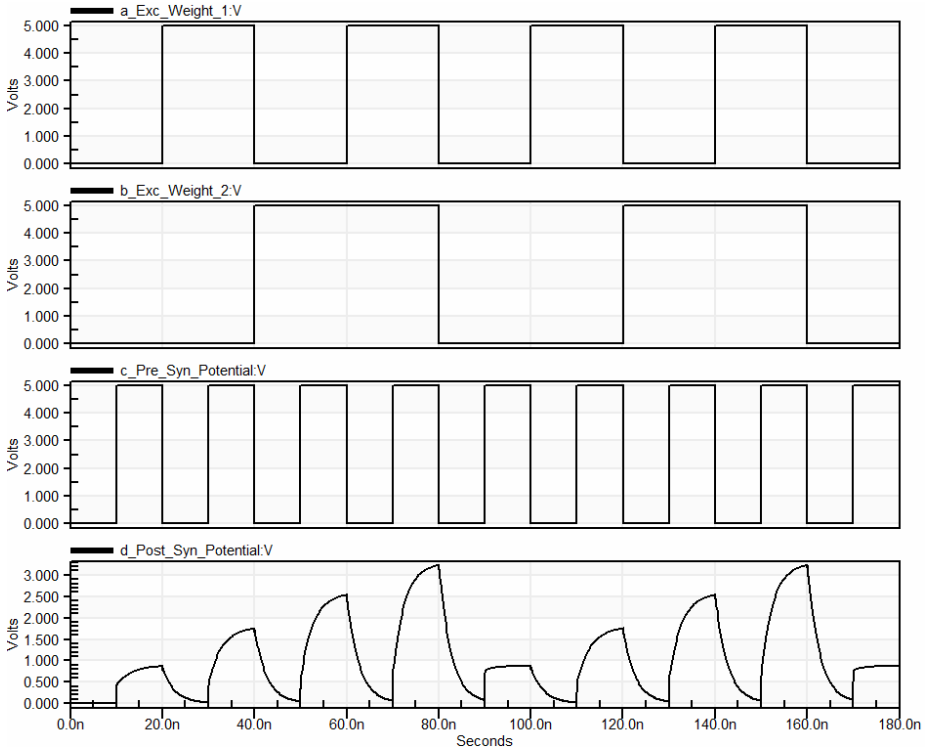

Figure 5 – Waveforms for input and output nodes of a synaptic input block

Neuron Activator and Spike Generator. A neuron fires spikes when the post-synaptic potential exceeds certain threshold value which serves as an action potential of the neuron. That is why as a neuron activator, Shmitt trigger may be applied. Shmitt trigger should convert an analog input signal (post-synaptic potential) to a digital output signal (command to activate spike generator). When the input is higher than a chosen threshold level, the output is the logical “1”, and when the input is below the threshold level the output is the logical “0”. A logical value is applied to the ring oscillator which serves as a generator of the neuron output. The ring oscillator is a simple circuit composed of an odd number of inverters connected in a ring. Circuit diagrams of Shmitt trigger and the ring oscillator used in the neuron circuit as activator and generator blocks are shown in Fig. 6.

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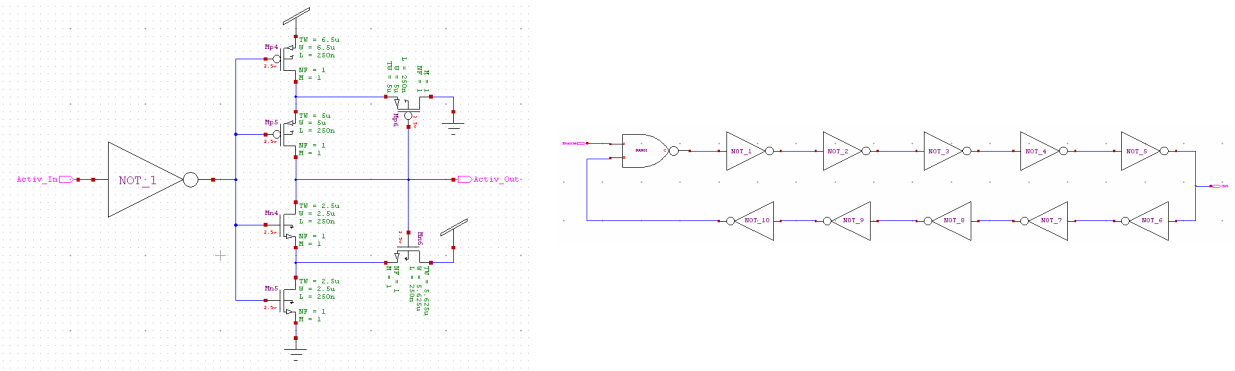

a) b)

Figure 6 – Circuit diagram of activator (a) and generator (b) blocks

Neuron Circuit Design and Functionality Verification. The functionality of the neuron is verified by the simulation of the neuron circuit shown in Fig. 7. The behavior of the neuron is simulated at various values of pre-synaptic input signals and 2-bit synaptic weights applied to the excitation and inhibitor circuits. In Fig. 8 it is shown waveforms of signals at key nodes of the neuron in the case when the excitation weight of the second synaptic input is twice the excitation weight of the first synaptic input, and the inhibitor weights at both inputs are not used. The threshold voltage level of the neuron activation potential is set by Schmitt trigger and is equal in this case to 2 V. The waveforms in Fig. 8 clearly show that when the total post-synaptic potential exceeds the activation potential, the neuron generates a sequence of pulses.

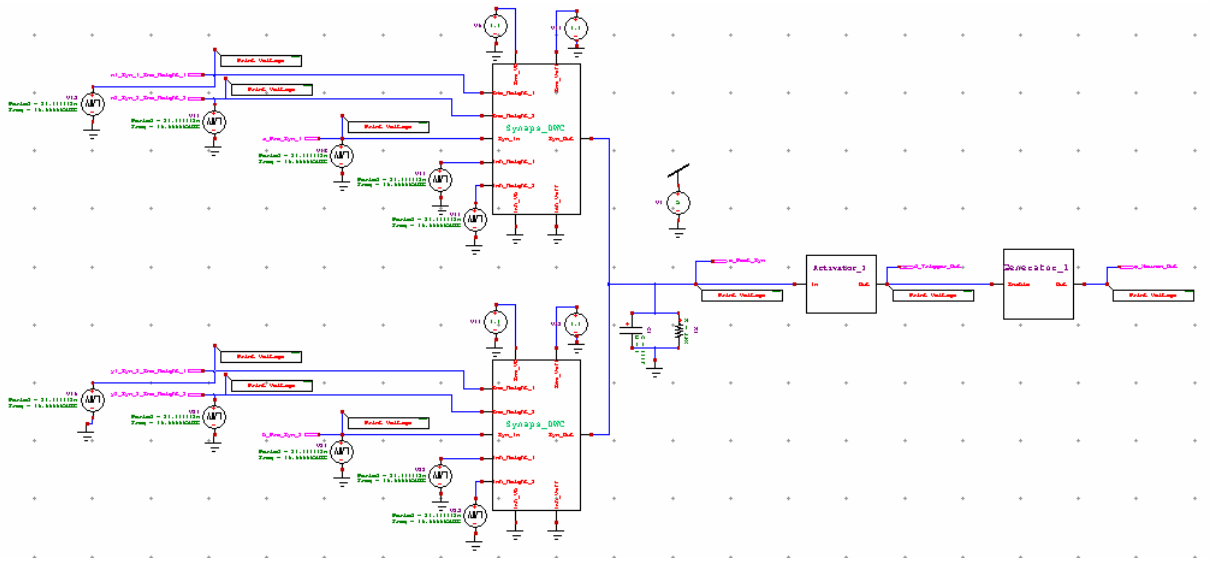

Figure 7 – Circuit diagram of the neuron

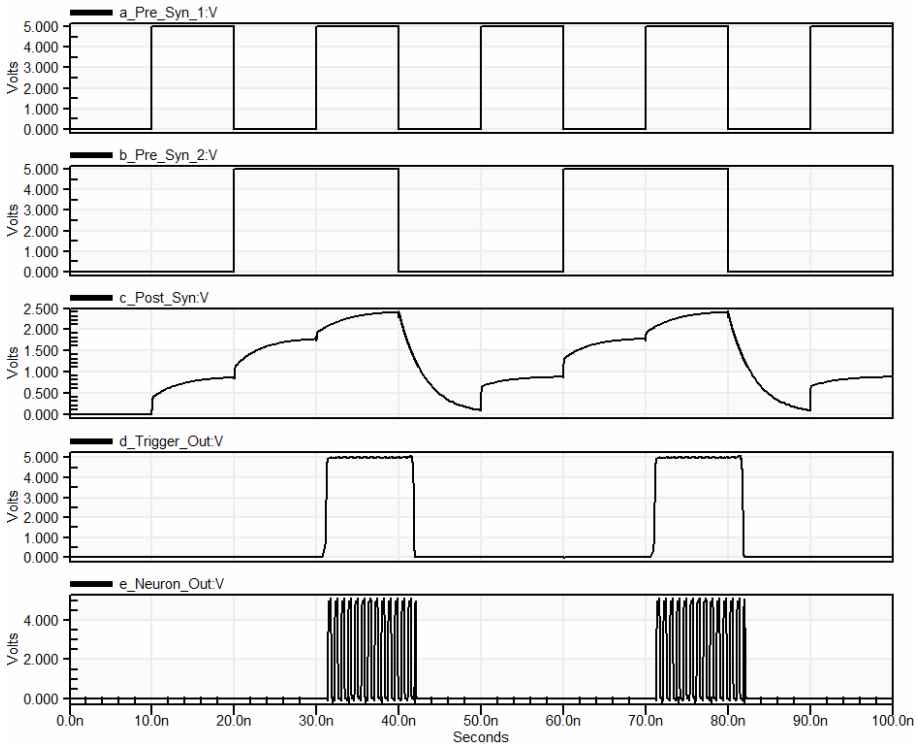

Figure 8 – Waveforms for signals at key nodes of the neuron

Conclusions. The hardware implementation of a spiking neuron has been designed for the application in spiking neural networks. The transistor level design has been performed using Leaky Integrate-and-Fire model of an artificial neuron with two synaptic inputs. To manage weight coefficients of the synaptic inputs, the digital weight control circuit has been designed which allows us to choose between four voltage levels of post synaptic potential using 2-bit numbers for synaptic weight coefficients. As a neuron activator, Shmitt trigger has been used to realize a threshold activation function and initiate a pulsed output by means of a ring oscillator. The design has been verified using EDA tool and signal waveforms at key nodes of the neuron have been obtained to demonstrate the neuron functionality.

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Проектування апаратної реалізації імпульсного нейрона

Апаратна реалізація штучного нейрона є ключовою проблемою створення нейроморфних чіпів, які являють собою нові перспективні архітектурні рішення для масово-паралельних обчислень. У цій статті представлено проектування аналогової схемної реалізації нейрона, який призначений для використання в якості базового елементу імпульсних нейронних мереж. Проектування виконано на транзисторному рівні з використанням LIF (Leaky Integrate-and-Fire) моделі нейрона. Нейрон моделювався і веріфікувався за допомогою інструментів автоматизованого проектування. Були отримані часові діаграми сигналів в ключових точках нейрона і продемонстрована його функціональність.

Hardware implementation design of a spiking neuron

The hardware implementation of an artificial neuron is the key problem of the design of neuromorphic chips which are new promising architectural solutions for massively parallel computing. In this paper an analog neuron circuit design is presented to be used as a building element of spiking neuron networks. The design of the neuron is performed at the transistor level based on Leaky Integrate-and-Fire neuron implementation model. The neuron is simulated using EDA tool to verify the design. Signal waveforms at key nodes of the neuron are obtained and neuron functionality is demonstrated.

The hardware implementation of a spiking neuron has been designed for the application in spiking neural networks. The transistor level design has been performed using Leaky Integrate-and-Fire model of an artificial neuron with two synaptic inputs. To manage weight coefficients of the synaptic inputs, the digital weight control circuit has been designed which allows us to choose between four voltage levels of post synaptic potential using 2-bit numbers for synaptic weight coefficients. As a neuron activator, Shmitt trigger has been used to realize a threshold activation function and initiate a pulsed output by means of a ring oscillator. The design has been verified using EDA tool and signal waveforms at key nodes of the neuron have been obtained to demonstrate the neuron functionality.

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